Feb. 2025

UniIC

SCE11U16320FF

16Gbit LPDDR4/4x SDRAM
RoHS Compliant Products

Data Sheet

Rev. A

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2025/02/28	A	Initial Release

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: info@unisemicon.com

Contents

1 Overview

This chapter gives an overview of the 16Gbit low power Double-Data-Rate-Four (LPDDR4/LPDDR4x) SDRAM component product and describes its main characteristics.

1.1 Features

The 16Gbit LPDDR4/LPDDR4x SDRAM offers the following key features:

- Density: 16Gbits
- Organization: 8Bank x 64Mbit x 16 x 2 Channel x 1 Ranks
- Data rate:4266/3733Mbps
- Ultra-low-voltage core and I/O power supplies
- – VDD1 = 1.70–1.95V; 1.80V nominal
- – VDD2 = 1.06–1.17V; 1.10V nominal
- – VDDQ = 0.57–0.65V; 0.60V nominal
- or VDDQ = 1.06–1.17V; 1.10V nominal
- Double-Data Rate Architecture
- Differential Clock Input (CK_t, CK_c)
- Bi-directional differential Data Strobe(DQS_t, DQS_c)
- Commands entered on both rising and falling positive CK edge; Data and Data Mask referenced to both edges of DQS_t
- DMI Pin
  - DBI (Data Bus Inversion) during normal Read and Write
  - Counting # of DQ's 1 for Masked Write when DBI on
  - DM (Data Mask) for Masked Write when DBI off
- 8 Internal Banks for each Channel
- Burst Length: 16, 32 and on-the-fly (OTF)
- Burst Type: Sequential
- Auto Precharge option for each Burst Access
- Configurable Drive Strength
- Refresh and Self Refresh mode
- Partial Array Self Refresh and Auto Temperature Compensated Self Refresh
- Write Leveling
- CA Calibration
- Internal VREF and VREF Training
- FIFO based Write/Read Training
- MPC (Multi-Purpose Command)
- LVSTLE (Low Voltage Swing Terminated Logic Extension) I/O
- VSSQ Termination
- Edge align Data Output; Write Training for Data Input Center align
- On-chip temperature sensor to control self-refresh rate
- Operating temperature range

  —-40℃ to +95℃

  —-40℃ to +105℃

1.2 Product List

Table 1 shows all possible products within the 16Gbit LPDDR4/LPDDR4x SDRAM component generation. Availability depends on application needs.

Table 1 - Ordering Information for 16Gbit LPDDR4/LPDDR4x SDRAM Components

Product Type1)	Org.	Speed	Clock (MHz)	Package	Note5)
Industrial Temperature Range (-40 °C~ +95 °C)					
LPDDR4x/4 3733M/4266M					
SCE11U16320FF-03AI	×32	LPDDR4x-3733	1866	200-Ball-FBGA	
SCE11U16320FF-04ZI	×32	LPDDR4x-4266	2133	200-Ball FBGA	
Automotive 3 Temperature Range (-40 °C~ +95 °C)					
LPDDR4x/4 3733M/4266M					
SCE11U16320FF-03AA3	×32	LPDDR4x-3733	1866	200-Ball FBGA	
SCE11U16320FF-04ZA3	×32	LPDDR4x-4266	2133	200-Ball FBGA	
Automotive 2 Temperature Range (-40 °C~ +105 °C)					
LPDDR4x/4 3733M/4266M					
SCE11U16320FF-03AA2	×32	LPDDR4x-3733	1866	200-Ball-FBGA	
SCE11U16320FF-04ZA2	×32	LPDDR4x-4266	2133	200-Ball FBGA	

1) CAS: Column Address Strobe.
2) RCD: Row Column Delay.
3) RP: Row Precharge.

1.3 Product Specification

1.3.1. General Description

The 16Gb mobile low-power DDR4 SDRAM with low VDDQ (LPDDR4/LPDDR4x) is a high-speed, CMOS dynamic random-access memory device. This device is internally configured with 1 channels x16 I/O having 8-banks.

1.3.2. General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQ collectively, unless stated otherwise.
DQS and CK should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless stated other- wise. CA includes all CA pins used for a given density.
In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[5:0]. VREF indicates VREFCA and VREFDQ.
Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements. Any specific requirement takes precedence over a general statement.
Any functionality not specifically stated herein is considered undefined, illegal, not supported, and will result in unknown operation.
For single-ended CK and DQS features or specifications, refer to the LPDDR4/LPDDR4x Single-Ended CK and DQS Addendum.

1.3.3. Device Configuration

Table 2-Device Configuration

		1G16 (16Gb/package)
Die organization in the package	Channel A, rank 0	x16 mode × 1 die (dual channel)
	Channel B, rank 0	
	Channel A, rank 1	–
	Channel B, rank 1	
	Channel A, rank 0, DQ[7:0]_A	–
	Channel A, rank 0, DQ[15:8]_A	–
	Channel A, rank 1, DQ[7:0]_A	–
	Channel A, rank 1, DQ[15:8]_A	–
	Channel B, rank 0, DQ[7:0]_B	–
	Channel B, rank 0, DQ[15:8]_B	–
	Channel B, rank 1, DQ[7:0]_B	–
	Channel B, rank 1, DQ[15:8]_B	–
Die addressing	Dual/single Die	dual-channel die
	Memory density (per die)	16Gb
	Memory density (per channel)	8Gb
	Configuration	64Mb × 16 DQ × 8 banks x 2channels
	Number of channels (per die)	2
	Number of banks (per channel)	8
	Array prefetch (bits, per channel)	256
	Number of rows (per channel)	65,536
	Number of columns (fetch boundaries)	64
	Page size (bytes)	2048
	Channel density (bits per channel)	8,589,934,592
	Total density (bits per die)	17,179,869,184
	Bank address	BA[2:0]
	Row address	R[15:0]
	Column address	C[9:0]
	Burst starting address boundary	64-bit

Notes: 1. Refer to Package Block Diagram section in Product Specification and SDRAM Addressing section in General LPDDR4X specification.

1.3.4. Refresh Requirement Parameters

Table 3- Refresh Requirement Parameters

Parameter	Symbol	8Gb Single-Channel Die	Unit
REFRESH cycle time (all banks)	tRFCab	280	ns
REFRESH cycle time (per bank)	tRFCpb	140	ns
Per bank refresh to per bank refresh time (different bank)	tPBR2PBR	90	ns

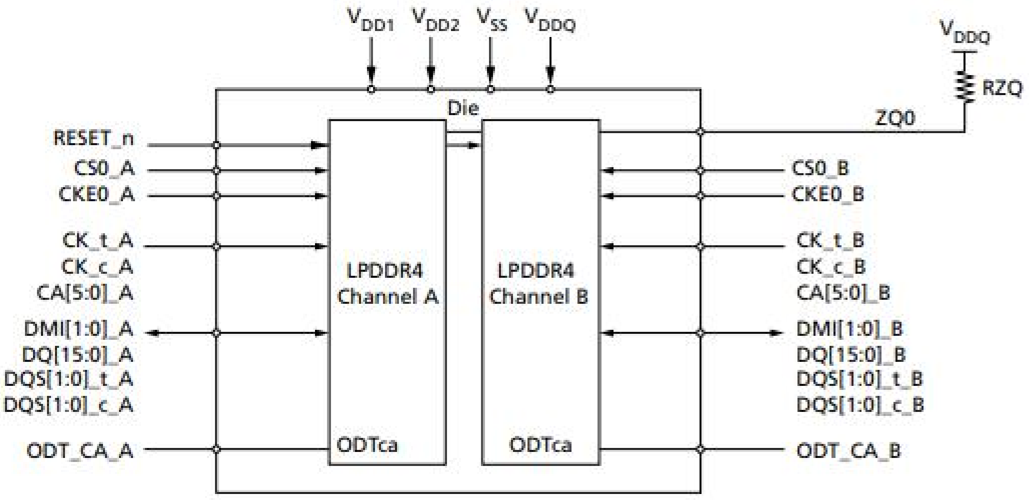
Notes: 1. This table only describes refresh parameters which are density dependent. Refer to Refresh Requirement section in General LPDDR4/4X specification for all the refresh parameters.

Table 4- Refresh Requirement Parameters (Continued)

Parameter		Symbol	Density (per channel)	Unit
			8Gb	
Number of banks per channel		–	8	–
Refresh window (tREFW): (1 × Refresh)3		tREFW	32	ms
Required number of REFRESH commands in tREFW window		R	8192	–
Average refresh interval (1 × Refresh)3	REFab	tREFI	3.906	µs
	REFpb	tREFIpb	488	ns
REFRESH cycle time (all banks)		tRFCab	280	ns
REFRESH cycle time (per bank)		tRFCpb	140	ns
Per bank refresh to per bank refresh time (different bank)		tPBR2PBR	90	ns

1.3.5. Package Block Diagrams

Figure 1-Single-Die, Dual-Channel, Single-Rank Package Block Diagram (x32 I/O)



1.3.6. Ball Assignments and Descriptions: 200-Ball

Table 5- Ball/Pad Descriptions

Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A, CKE0_B,	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A,CS0_B,	Input	**Chip select:** Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	**LPDDR4 CA ODT control:** The ODT_CA pin is used in conjunction with the mode registerto turn on/off the on-die termination for CA pins. It is bonded to V_{DD2} within the package, or at the package ball, for the terminating rank, and the non-terminating ranks arebonded to V_{SS} (or left floating with a weak pull-down on the DRAM die). The terminatingrank is the DRAM that terminates the CA bus for all die on the same channel. **LPDDR4X CA ODT Control:** The ODT_CA pin is ignored by LPDDR4X devices. CA ODT isfully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data input/output:** Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Data strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data mask/Data bus inversion:** Data mask inversion (DMI) is a dual use bi-directional sig-nal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode reg-ister setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0, ZQ1	Refer- ence	**ZQ calibration reference:** Used to calibrate the output drive strength and the termina-tion resistance. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET pin resets all channels of the die.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.

200-Ball FBGA (x16,2Ch configuration)

Figure 2- 200-Ball Dual-Channel, Single-Rank Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V_{SS}	V_{DD2}	ZQ0			NC	V_{DD2}	V_{SS}	DNU	DNU
B	DNU	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	DNU
C	V_{SS}	DQ1_A	DMI0_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DMI1_A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_t_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2_A	DQS0_c_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_c_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11_A	V_{DD1}
G	V_{SS}	ODT_CA_A	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	NC	V_{SS}
H	V_{DD2}	CA0_A	NC	CS0_A	V_{DD2}			V_{DD2}	CA2_A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1_A	V_{SS}	CKE0_A	NC			CK_t_A	CK_c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	CA1_B	V_{SS}	CKE0_B	NC			CK_t_B	CK_c_B	V_{SS}	CA5_B	V_{SS}
R	V_{DD2}	CA0_B	NC	CS0_B	V_{DD2}			V_{DD2}	CA2_B	CA3_B	CA4_B	V_{DD2}
T	V_{SS}	ODT_CA_B	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	DQ3_B	V_{DDQ}	DQ4_B	V_{DD2}			V_{DD2}	DQ12_B	V_{DDQ}	DQ11_B	V_{DD1}
V	V_{SS}	DQ2_B	DQS0_c_B	DQ5_B	V_{SS}			V_{SS}	DQ13_B	DQS1_c_B	DQ10_B	V_{SS}
W	V_{DDQ}	V_{SS}	DQS0_t_B	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_B	V_{SS}	V_{DDQ}
Y	V_{SS}	DQ1_B	DMI0_B	DQ6_B	V_{SS}			V_{SS}	DQ14_B	DMI1_B	DQ9_B	V_{SS}
AA	DNU	DQ0_B	V_{DDQ}	DQ7_B	V_{DDQ}			V_{DDQ}	DQ15_B	V_{DDQ}	DQ8_B	DNU
AB	DNU	DNU	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12

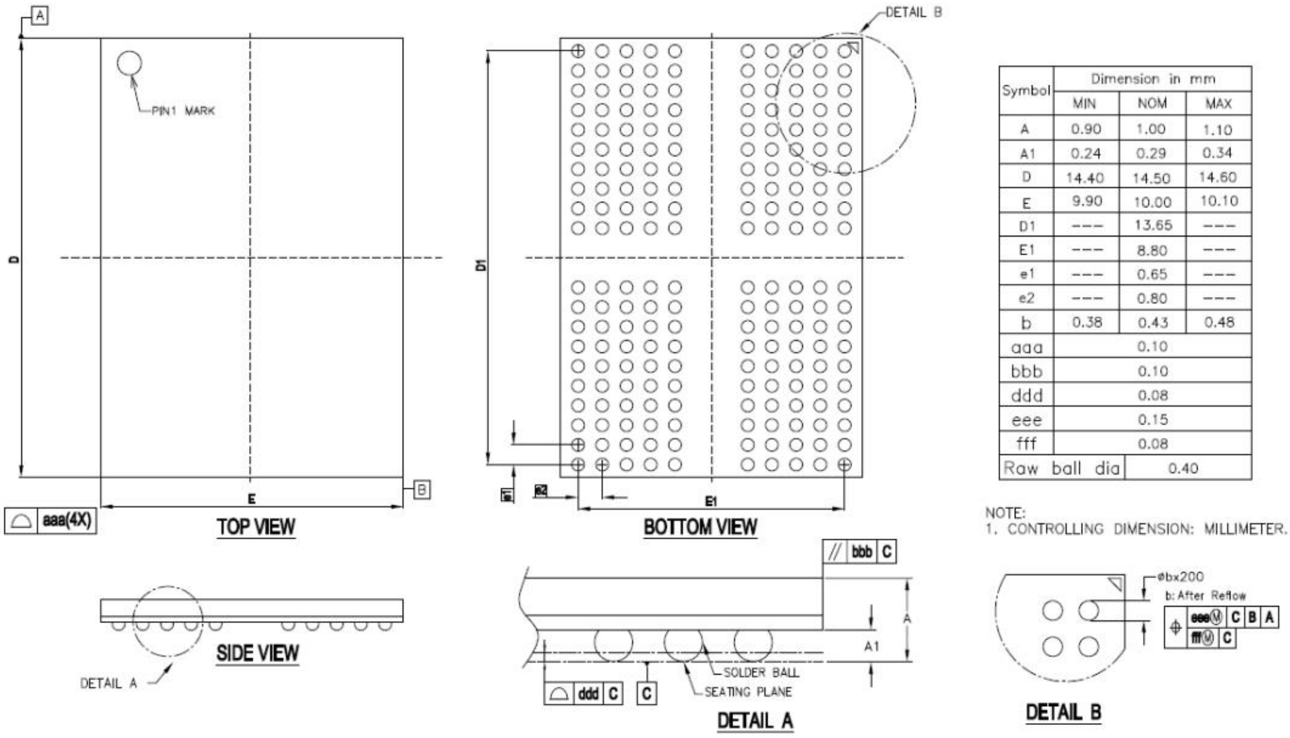
Top View (ball down)

LPDDR4_A (Channel A) LPDDR4_B (Channel B) ZQ, ODT_CA, RESET Supply Ground

1.3.7. Package Diagram

200-Ball Fine Pitch Ball Grid Array Outline

Figure 3-200-Ball TFBGA （10mm x 14.5mm x 1.1mm max）



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.24	0.29	0.34
D	14.40	14.50	14.60
E	9.90	10.00	10.10
D1	---	13.65	---
E1	---	8.80	---
e1	---	0.65	---
e2	---	0.80	---
b	0.38	0.43	0.48
aaa		0.10	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.08	
Raw ball dia		0.40	

Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 with NiAu pads (Sn3.0Ag0.5Cu).

2 Functional Description

2.1. Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be either reset by asserting the RESET_n command or powered down and then restarted using the specified initialization sequence before normal operation can continue.

CKE signal has to be held HIGH when the commands listed in the command truth table input.

Table 6- Command Truth Table

Command	CS	SDR CA Pins						CK Edge	Notes
		CA0	CA1	CA2	CA3	CA4	CA5		
MRW-1	H	L	H	H	L	L	OP7	1	1, 11
	L	MA0	MA1	MA2	MA3	MA4	MA5	2	
MRW-2	H	L	H	H	L	H	OP6	1	1, 11
	L	OP0	OP1	OP2	OP3	OP4	OP5	2	
MRR-1	H	L	H	H	H	L	V	1	1, 2, 12
	L	MA0	MA1	MA2	MA3	MA4	MA5	2	
REFRESH (all/per bank)	H	L	L	L	H	L	AB	1	1, 2, 3, 4
	L	BA0	BA1	BA2	V	V	V	2	
ENTER SELF REFRESH	H	L	L	L	H	H	V	1	1, 2
	L	V						2	
ACTIVATE-1	H	H	L	R12	R13	R14	R15	1	1, 2, 3, 10
	L	BA0	BA1	BA2	R16	R10	R11	2	
ACTIVATE-2	H	H	H	R6	R7	R8	R9	1	1, 10
	L	R0	R1	R2	R3	R4	R5	2	
WRITE-1	H	L	L	H	L	L	BL	1	1, 2, 3, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	2	
EXIT SELF REFRESH	H	L	L	H	L	H	V	1	1, 2
	L	V						2	
MASK WRITE-1	H	L	L	H	H	L	BL	1	1, 2, 3, 5, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	2	
RFU	H	L	L	H	H	H	V	1	1, 2
	L	V						2	
RFU	H	L	H	L	H	L	V	2	1, 2
	L	V						2	
RFU	H	L	H	L	H	H	V	2	1, 2
	L	V						2	
READ-1	H	L	H	L	L	L	BL	1	1, 2, 3, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	2	
CAS-2 (WRITE-2, MASKED WRITE-2, READ-2, MRR-2, MPC (except NOP)	H	L	H	L	L	H	C8	1	1, 8, 9
	L	C2	C3	C4	C5	C6	C7	2	
PRECHARGE (all/per bank)	H	L	L	L	L	H	AB	1	1, 2, 3, 4
	L	BA0	BA1	BA2	V	V	V	2	

Table 5- Command Truth Table (Continued)

Command	CS	SDR CA Pins						CK Edge	Notes
		CA0	CA1	CA2	CA3	CA4	CA5		
MPC (TRAIN, NOP)	H	L	L	L	L	L	OP6	↑1	1, 9, 13
	L	OP0	OP1	OP2	OP3	OP4	OP5	↑2	
DESELECT	L	X						↑1	1, 2

Notes:
1. All commands except for DESELECT are two clock cycles and are defined by the current state of CS and CA[5:0] at the rising edge of the clock. DESELECT command is one clock cycle and is not latched by the device.
2. V = H or L (a defined logic level); X = "Don't Care," in which case CS, CK_t, CK_c, and CA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB HIGH during PRECHARGE or REFRESH commands indicate the command must be applied to all banks, and the bank addresses are "Don't Care."
5. MASK WRITE-1 command only supports BL16. For MASK WRITE-1 commands, CA5 must be driven LOW on the first rising clock cycle (R1).
6. AP HIGH during a WRITE-1, MASK WRITE-1, or READ-1 command indicates that an auto precharge will occur to the bank the command is operating on. AP LOW indicates that no auto precharge will occur and the bank will remain open upon completion of the command.
7. When enabled in the mode register, BL HIGH during a WRITE-1, MASK-WRITE-1, or READ-1 command indicates the burst length should be set on-the-fly to BL = 32; BL LOW during one of these commands indicates the burst length should be set on-the-fly to BL = 16. If on-the-fly burst length is not enabled in the mode register, this bit should be driven to a valid level and is ignored by the device.
8. For CAS-2 commands (WRITE-2, MASK WRITE-2, READ-2, MRR-2, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION)), C[1:0] are not transmitted on the CA [5:0] bus and are assumed to be zero. Note that for CAS-2 WRITE-2 or CAS-2 MASK WRITE-2 command, C[3:2] must be driven LOW.
9. WRITE-1, MASK-WRITE-1, READ-1, MODE REGISTER READ-1, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION) command must be immediately followed by CAS-2 command consecutively without any other command in between. WRITE-1, MASK WRITE-1, READ-1, MRR-1, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION) command must be issued first before issuing CAS-2 command. MPC (only START and STOP DQS OSCILLATOR, ZQCAL START and LATCH) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10. The ACTIVATE-1 command must be followed by the ACTIVATE-2 command consecutively without any other command between them. The ACTIVATE-1 command must be issued prior to the ACTIVATE-2 command. When the ACTIVATE-1 command is issued, the ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.
11. The MRW-1 command must be followed by the MRW-2 command consecutively without any other command between them. The MRW-1 command must be issued prior to the MRW-2 command.
12. The MRR-1 command must be followed by the CAS-2 command consecutively without any other commands between them. The MRR-1 command must be issued prior to the CAS-2 command.
13. The MPC command for READ or WRITE TRAINING operations must be followed by the CAS-2 command consecutively without any other commands between them. The MPC command must be issued prior to the CAS-2 command.
14. Commands are transmitted to the device across a six-lane interface and use CK, CKE, and CS to control the capture of transmitted data.

2.2 Power-up Initialization Sequence

To ensure proper functionality for power-up and reset initialization, default values for the MR settings are provided in the table below.

Table 7- Mode register Default Settings for LPDDR4x

Item	Mode Register Setting	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00b	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0b	WRITE latency set A is selected

WL	MR2 OP[5:3]	000b	WL = 4
RL	MR2 OP[2:0]	000b	RL = 6, *n*RTP = 8
*n*WR	MR1 OP[6:4]	000b	*n*WR = 6
DBI-WR/RD	MR3 OP[7:6]	00b	Write and read DBI are disabled
CA ODT	MR11 OP[6:4]	000b	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000b	DQ ODT is disabled
VREF(CA) setting	MR12 OP[6]	1b	VREF(CA) range[1] is enabled
VREF(CA) value	MR12 OP[5:0]	011101b	Range1: 50.3% of VDDQ
VREF(DQ) setting	MR14 OP[6]	1b	VREF(DQ) range[1] enabled
VREF(DQ) value	MR14 OP[5:0]	011101b	Range1: 50.3% of VDDQ

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory. The power-up sequence of all channels must proceed simultaneously.

Table 8- Mode register Default Settings for LPDDR4

This section defines LPDDR4 specifications to enable 1.10 VDDQ operation of LPDDR4 devices.

Item	Mode Register Setting	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00b	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0b	WRITE latency set A is selected
WL	MR2 OP[5:3]	000b	WL = 4
RL	MR2 OP[2:0]	000b	RL = 6, *n*RTP = 8
*n*WR	MR1 OP[6:4]	000b	*n*WR = 6
DBI-WR/RD	MR3 OP[7:6]	00b	Write and read DBI are disabled
CA ODT	MR11 OP[6:4]	000b	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000b	DQ ODT is disabled
VREF(CA) setting	MR12 OP[6]	1b	VREF(CA) range[1] is enabled
VREF(CA) value	MR12 OP[5:0]	001101b	Range1: 27.2% of VDDQ
VREF(DQ) setting	MR14 OP[6]	1b	VREF(DQ) range[1] enabled
VREF(DQ) value	MR14 OP[5:0]	001101b	Range1: 27.2% of VDDQ

2.2.1. Voltage Ramp

1.While applying power (after Ta), RESET_n should be held LOW (≤0.2 × VDD2), and all other inputs must be between VIL,min and VIH,max. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the table below. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table 9- Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

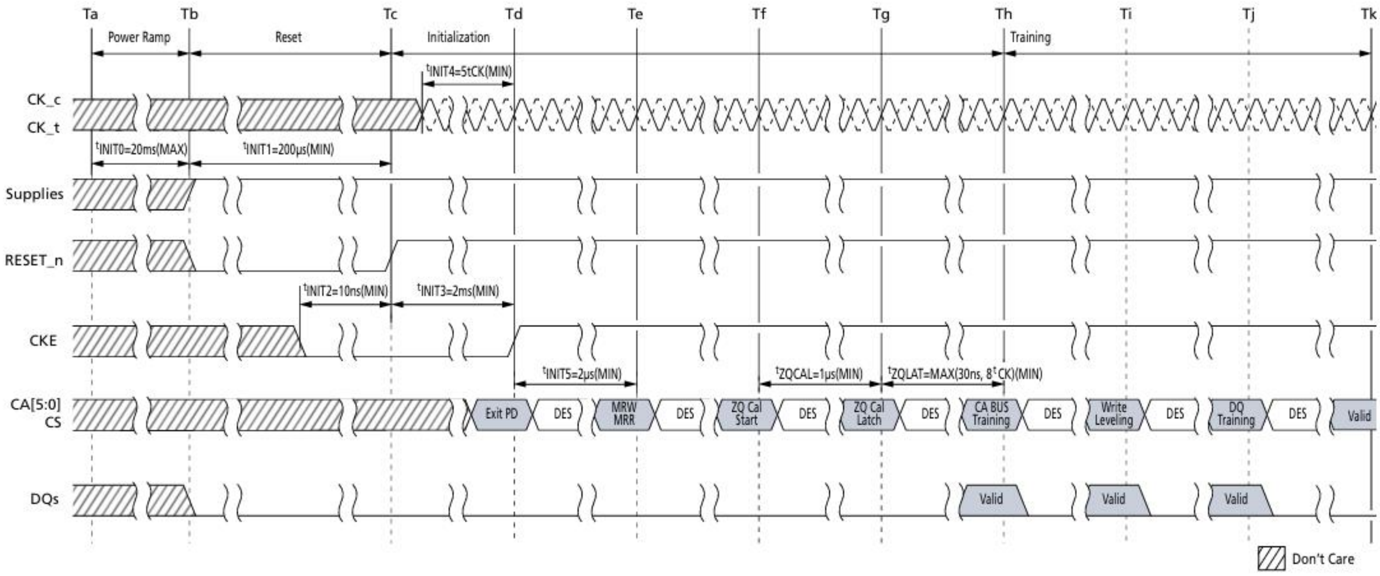
Notes: 1. Ta is the point when any power supply first reaches 300mV.

2. Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operating ranges.
4. Power ramp duration tINIT0 (Tb–Ta) must not exceed 20ms.
5. The voltage difference between any VSS and VSSQ must not exceed 100mV.

2.Following completion of the voltage ramp (Tb), RESET_n must be held LOW for tINIT1. DQ, DMI,DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK_t and CK_c, CS, and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in the table below.

3.Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care.

Figure 4-Voltage Ramp and Initialization Sequence



Note: 1. Training is optional and may be done at the system designer's discretion. The order of training may be different than what is shown here.

4.After RESET_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. CK_t, CK_c must be started and stabilized for tINIT4 before CKE goes active(Td). CS must remain LOW when the controller activates CKE.

5.After CKE is set to HIGH, wait a minimum of tINIT5 to issue any MRR or MRW commands(Te). For MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6.After completing all MRW commands to set the pull-up, pull-down, and Rx termination values, the controller can issue the ZQCAL START command to the memory(Tf). This command is used to calibrate the VOH level and the output impedance over process, voltage, and temperature. In systems where more than one device share one external ZQ resistor, the controller must not overlap the ZQ cali- bration sequence of each device. The ZQ calibration sequence is completed after tZQCAL (Tg). The ZQCAL LATCH command must be issued to update the DQ drivers and DQ + CA ODT to the calibrated values.

7.After tZQLAT is satisfied (Th), the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (command bus training mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The device will power-up with receivers configured for low-speed operations and with VREF(CA) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training is complete. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and it outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.

8.After command bus training, the controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is HIGH(Ti). See the Write Leveling section for a detailed description of the write leveling entry and exit sequence. In write leveling mode, the controller adjusts write DQS timing to the point where the device recognizes the start of write DQ data burst with desired WRITE latency.

9.After write leveling, the DQ bus (internal VREF(DQ), DQS, and DQ) should be trained for high-speed operation using the MPC TRAINING commands and by issuing MRW commands to adjust VREF(DQ). The device will power-up with receivers configured for low-speed operations and with VREF(DQ) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ bus training is complete. The MPC[READ DQ CALIBRATION] command is used together with MPC[READ-FIFO] or MPC[WRITE-FIFO] commands to train the DQ bus without disturbing the memory array contents. See the DQ Bus Training section for more information on the DQ bus training sequence.

10.At Tk, the device is ready for normal operation and is ready to accept any valid command. Any mode registers that have not previously been configured for normal operation should be written at this time.

Table 10-Initialization Timing Parameters

Parameter	Min	Max	Unit	Comment
tINIT0	–	20	ms	Maximum voltage ramp time
tINIT1	200	–	μs	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	–	ns	Minimum CKE LOW time before RESET_n goes HIGH
tINIT3	2	–	ms	Minimum CKE LOW time after RESET_n goes HIGH
tINIT4	5	–	tCK	Minimum stable clock before first CKE HIGH
tINIT5	2	–	μs	Minimum idle time before first MRW/MRR command
tCKb	Note[1,2]	Note[1, 2]	ns	Clock cycle time during boot

Notes: 1. Minimum tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by minimum tCKb. The higher boot frequency is system dependent.

2.3 Mode Registers

2.3.1. Mode Register Assignments and Definitions

Mode register definitions are provided in the Mode Register Assignments table. In the access column of the table, R indicates read-only; W indicates write-only; R/W indicates read- or write-capable or enabled. The MRR command is used to read from a register. The MRW command is used to write to a register.

Table 11- Mode Register Assignments

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device info	R	RFU			RZQI		RFU	Latency mode	REF
1	01h	Device feature 1	W	RD-PST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	02h	Device feature 2	W	WR Lev	WLS	WL			RL		
3	03h	I/O config-1	W	DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL
4	04h	Refresh and training	R /W	TUF	Thermal offset		PPRE	SR abort	Refresh rate		
5	05h	Basic config-1	R	Manufacturer ID							
6	06h	Basic config-2	R	Revision ID1							
7	07h	Basic config-3	R	Revision ID2							
8	08h	Basic config-4	R	I/O width		Density				Type	
9	09h	Test mode	W	Vendor-specific test mode							
10	0Ah	I/O calibration	W	RFU							ZQ RST
11	0Bh	ODT	W	RFU	CA ODT			RFU	DQ ODT		
12	0Ch	VREF(CA)	R/W	RFU	VRCA	VREF(CA)					
13	0Dh	Register control	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	0Eh	VREF(DQ)	R/W	RFU	VRDQ	VREF(DQ)					
15	0Fh	DQI-LB	W	Lower-byte invert register for DQ calibration							
16	10h	PASR_Bank	W	PASR bank mask							
17	11h	PASR_Seg	W	PASR segment mask							
18	12h	IT-LSB	R	DQS oscillator count – LSB							
19	13h	IT-MSB	R	DQS oscillator count – MSB							
20	14h	DQI-UB	W	Upper-byte invert register for DQ calibration							
21	15h	Vendor use	W	RFU							
22	16h	ODT feature 2	W	ODTD for x8_2ch		ODTD -CA	ODTE -CS	ODTE -CK	SoC ODT		
23	17h	DQS oscillator stop	W	DQS oscillator run-time setting							

Table10 - Mode Register Assignments (Continued)

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
24	18h	TRR control when MR0 OP2 = 0b	R/W	TRR mode	TRR mode BAn			Unltd MAC	MAC value		
		TRR control when MR0 OP2 = 1b	R	RAAMMT		RAAIMT					RFM
25	19h	PPR resources	R	B7	B6	B5	B4	B3	B2	B1	B0
26–29	1Ah–1Dh	–	–	Reserved for future use							
30	1Eh	Reserved for test	W	SDRAM will ignore							
31	1Fh	–	–	Reserved for future use							
32	20h	DQ calibration pattern A	W	See DQ calibration section							
33–35	21h–23h	Do not use	–	Do not use							
36	24h	RAADEC	R	RFU						RAADEC	
37-38	25h-26h	Do not use	–	Do not use							
39	27h	Reserved for test	W	SDRAM will ignore							
40	28h	DQ calibration pattern B	W	See DQ calibration section							
41-47	29h-2Fh	Do not use	–	Do not use							
48-63	30h-3Fh	Reserved	–	Reserved for future use							

Notes:
1. RFU bits must be set to 0 during MRW commands.
2. RFU bits are read as 0 during MRR commands.
3. All mode registers that are specified as RFU or write-only shall return undefined data when read via an MRR command.
4. RFU mode registers must not be written.
5. Writes to read-only registers will not affect the functionality of the device.
6. Notes 1–5 apply to entire table.

2.4 Refresh command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of clock. Per-bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. The all-bank REFRESH is initiated with CA5 HIGH at the first rising edge of clock.

A per-bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1, and CA2 on the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1, and bank address BA2 is transferred on CA2. A per-bank REFRESH command (REFpb) to the eight banks can be issued in any order. For example, REFpb commands may be issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per-bank REFRESH command, the controller can send another set of per-bank REFRESH commands in the same order or a different order. One possible order can be a sequential round robin:
0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all eight banks have been refreshed using the per-bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the device by resetting the bank count to zero. Synchronization can occur upon reset procedure or at every exit from self refresh. The REFab command also synchronizes the counter between the controller and the device to zero. The device can be placed in self refresh, or a REFab command can be issued at any time without cycling through all eight banks using per-bank REFRESH command. After the bank count is synchronized to zero, the controller can issue per-bank REFRESH commands in any order, as described above.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the device will perform refreshes to all banks as indicated by the row counter. If another REFRESH command (REFab or REFpb) is issued after the REFab command then it uses an incremented value of the row counter.

The table below shows examples of both bank and refresh counter increment behavior.

Table 12 - Bank and Refresh Counter Increment Behavior

#	Command	BA2	BA1	BA0	Refresh Bank #	Bank Counter #	Ref. Conter # (Row Address #)
0	Reset, SRX, or REFab					To 0	–
1	REFpb	0	0	0	0	0 to 1	n
2	REFpb	0	0	1	1	1 to 2	
3	REFpb	0	1	0	2	2 to 3	
4	REFpb	0	1	1	3	3 to 4	
5	REFpb	1	0	0	4	4 to 5	
6	REFpb	1	0	1	5	5 to 6	
7	REFpb	1	1	0	6	6 to 7	
8	REFpb	1	1	1	7	7 to 0	
9	REFpb	1	1	0	6	0 to 1	n + 1
10	REFpb	1	1	1	7	1 to 2	
11	REFpb	0	0	1	1	2 to 3	
12	REFpb	0	1	1	3	3 to 4	
13	REFpb	1	0	1	5	4 to 5	
14	REFpb	0	1	0	2	5 to 6	
15	REFpb	0	0	0	0	6 to 7	
16	REFpb	1	0	0	4	7 to 0	
17	REFpb	0	0	0	0	0 to 1	n + 2
18	REFpb	0	0	1	1	1 to 2	
19	REFpb	0	1	0	2	2 to 3	
20	**REFab**	**V**	**V**	**V**	**0 to 7**	**To 0**	**n + 2**
21	REFpb	1	1	0	6	0 to 1	n + 3
22	REFpb	1	1	1	7	1 to 2	
Snip							

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after the prior PRECHARGE command to that bank
- tRRD has been satisfied after the prior ACTIVATE command (for example, after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time (tRFCpb). However, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command

- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank
- tRFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to every bank in a channel. All banks must be idle when REFab is issued (for example, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command
- tRFCpb has been satisfied following the prior REFpb command
- tRP has been satisfied following the prior PRECHARGE command

When an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- RFCab latency must be satisfied before issuing an ACTIVATE command,
- RFCab latency must be satisfied before issuing a REFab or REFpb command

Table 13 - REFRESH Command Timing Constraints

Symbol	Minimum Delay From...	To	Notes
tRFCab	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		-REFpb	
tRRD	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Notes: 1. A bank must be in the idle state before it is refreshed; therefore, REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

Figure 5-All-Bank REFRESH Operation

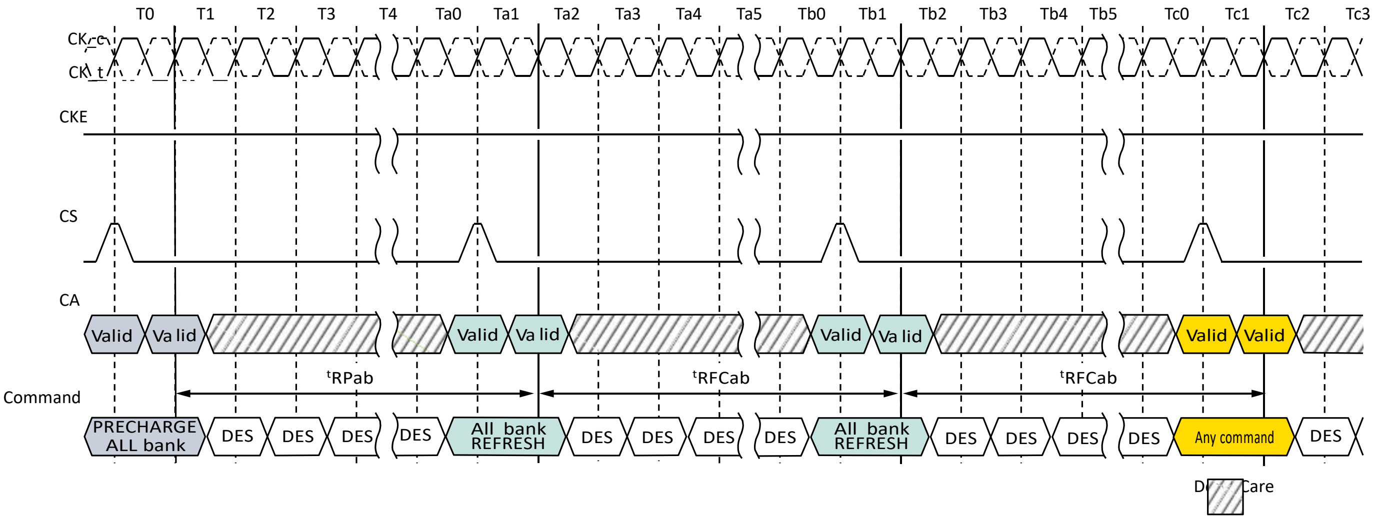
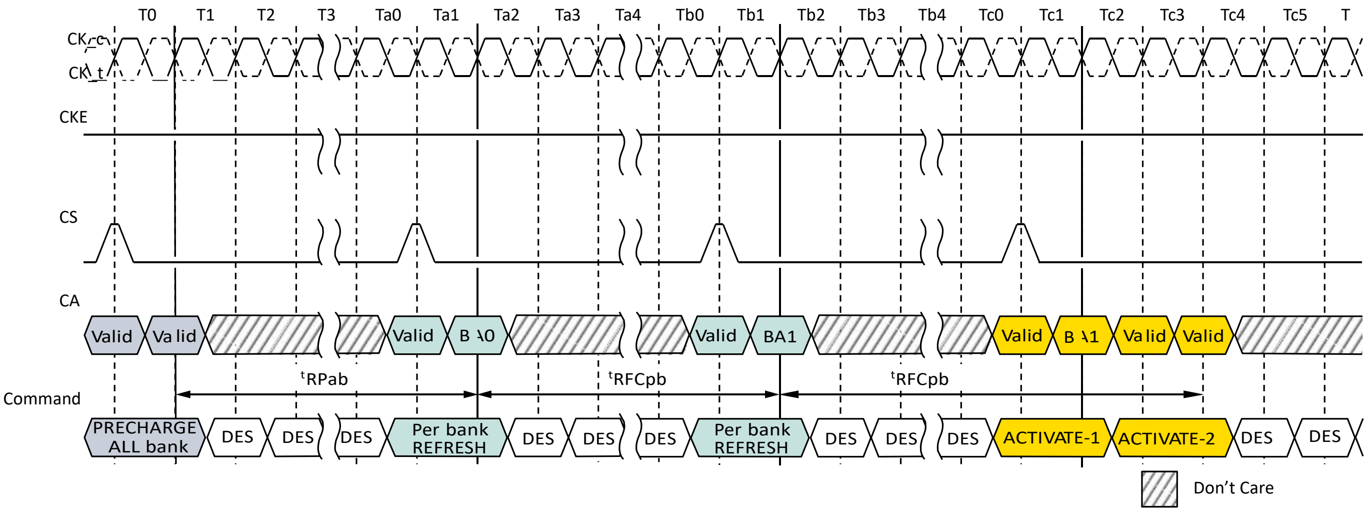


Figure 6- Per-Bank REFRESH Operation



Notes: 1. In the beginning of this example, the REFpb bank is pointing to bank 0.
2. Operations to banks other than the bank being refreshed are supported during the tRFCpb period.

In general, a REFRESH command needs to be issued to the device regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be postponed during operation of the device, but at no point in time are more than a total of eight REFRESH commands allowed to be postponed. And a maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in the table below. In the case where eight REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to 9 × tREFI. A maximum of eight additional REFRESH commands can be issued in advance (pulled in), with each one reducing the number of regular REFRESH commands required later by one. Note that pulling in more than eight REFRESH commands in advance does not reduce the number of regular REFRESH commands required later; therefore, the resulting maximum interval between two surrounding REFRESH commands is limited to 9 × t REFI. At any given time, a maximum of 16 REFRESH commands can be issued within 2 × t REFI.

Self-refresh mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting self-refresh mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed to the extent that the total number of postponed REFRESH commands (before and after self-refresh) will never exceed eight. During self-refresh mode, the number of postponed or pulled-in REFRESH commands does not change.

And for per-bank refresh, a maximum of 8 x 8 per-bank REFRESH commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 x 8 x 8 per-bank REFRESH commands can be issued within 2 × tREFI.

Table 14 - Legacy REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh rate	Max. No. of pulled-in or postponed REFab	Max. Interval between two REFab	Max. No. of REFab1	Per-bank REFRESH
000b	Low temp. limit	N/A	N/A	N/A	N/A
001b	4 × tREFI	8	9 × 4 × tREFI	16	1/8 of REFab
010b	2 × tREFI	8	9 × 2 × tREFI	16	1/8 of REFab
011b	1 × tREFI	8	9 × tREFI	16	1/8 of REFab
100b	0.5 × tREFI	8	9 × 0.5 × tREFI	16	1/8 of REFab
101b	0.25 × tREFI	8	9 × 0.25 × tREFI	16	1/8 of REFab
110b	0.25 × tREFI	8	9 × 0.25 × tREFI	16	1/8 of REFab
111b	High temp. limit	N/A	N/A	N/A	N/A

Note: 1. Maximum number of REFab within MAX(2 × tREFI × refresh rate multiplier, 16 × tRFC).

Table 15- Modified REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh Rate	Max. No. of Pulled-in or Postponed REFab	Max. Interval between Two REFab	Max. No. of REFab1	Per-bank REFRESH
000B	Low temp. limit	N/A	N/A	N/A	N/A
001B	4 × tREFI	2	3 × 4 × tREFI	4	1/8 of REFab
010B	2 × tREFI	4	5 × 2 × tREFI	8	1/8 of REFab
011B	1 × tREFI	8	9 × tREFI	16	1/8 of REFab
100B	0.5 × tREFI	8	9 × 0.5 × tREFI	16	1/8 of REFab
101B	0.25 × tREFI	8	9 × 0.25 × tREFI	16	1/8 of REFab
110B	0.25 × tREFI	8	9 × 0.25 × tREFI	16	1/8 of REFab
111B	High temp. limit	N/A	N/A	N/A	N/A

Notes: 1. For any thermal transition phase where refresh mode is transitioned to either 2 × tREFI or 4 × tREFI, LPDDR4/4x devices will support the previous postponed refresh requirement provided the number of postponed refreshes is mono- tonically reduced to meet the new requirement. However, the pulled-in REFRESH commands in the previous thermal phase are not applied in the new thermal phase. Entering a new thermal phase, the controller must count the number of pulled-in REFRESH commands as zero, regardless of the number of remaining pulled-in REFRESH commands in the previous thermal phase.

2. LPDDR4/4x devices are refreshed properly if the memory controller issues REFRESH commands with same or shorter refresh period than reported by MR4 OP[2:0]. If a shorter refresh period is applied, the corresponding require- ments from this table apply. For example, when MR4 OP[2:0] = 001b, the controller can be in any refresh rate from 4 × tREFI to 0.25 × tREFI. When MR4 OP[2:0] = 010b, the only prohibited refresh rate is 4 × tREFI.

Figure 7-Postponing REFRESH Commands (Example)

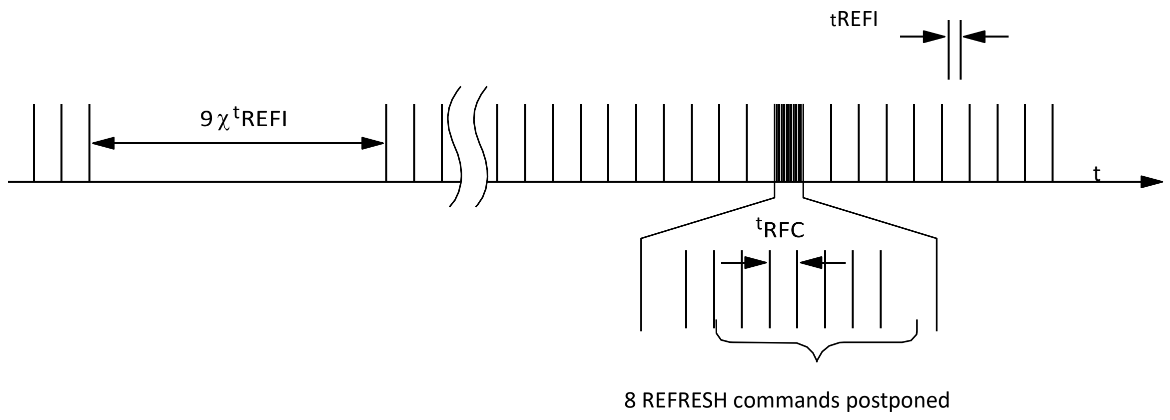
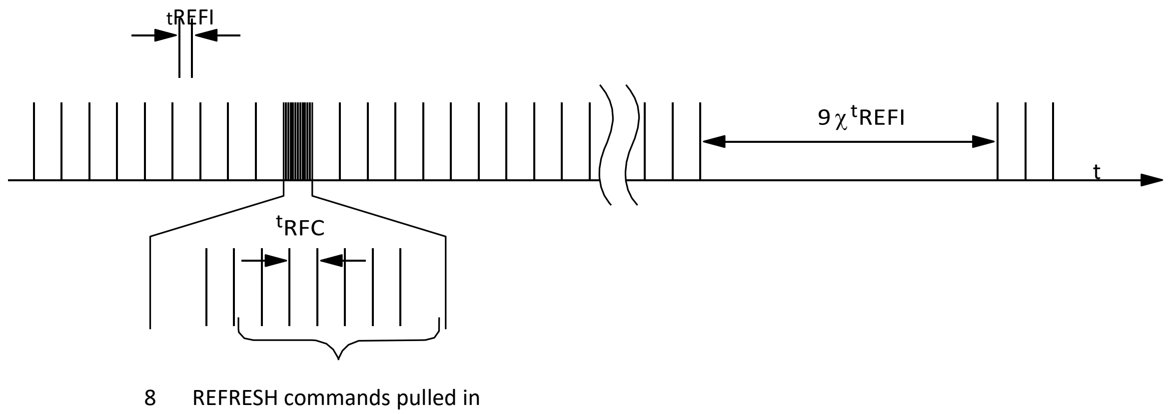
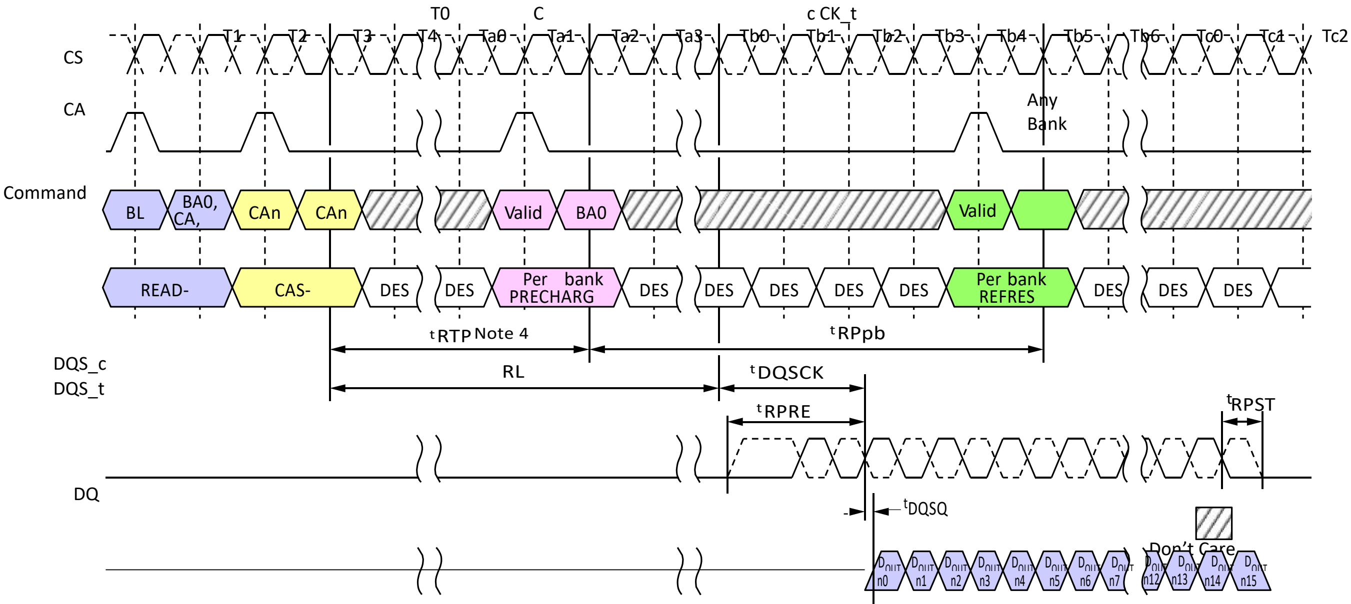


Figure 8-Pulling in REFRESH Commands (Example)



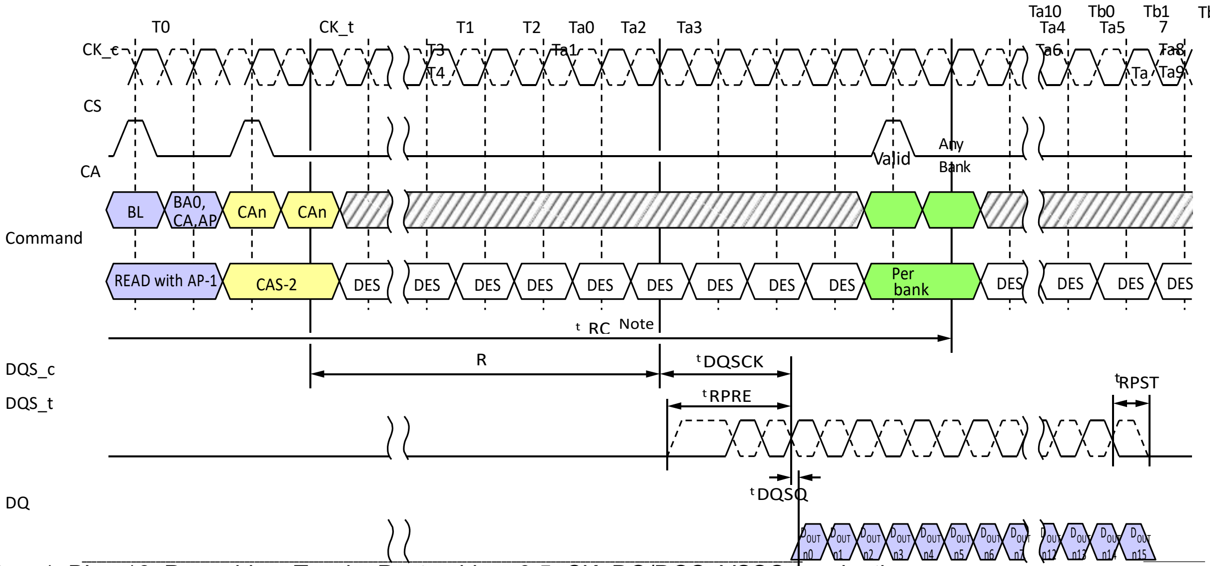
2.4.1. Burst READ Operation Followed by Per-Bank Refresh

Figure 9-Burst READ Operation Followed by Per-Bank Refresh



Notes: 1. The per-bank REFRESH command can be issued after tRTP + tRPpb from READ command.
2. BL = 16; Preamble = Toggle; Postamble = 0.5nCK; DQ/DQS: VSSQ termination.
3. DOUT n = data-out from column n.
4. In the case of BL = 32, delay time from read to per-bank precharge is 8nCK + tRTP.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 10-Burst READ With AUTO PRECHARGE Operation Followed by Per-Bank Refresh



Notes: 1. BL = 16; Preamble = Toggle; Postamble = 0.5*n*CK; DQ/DQS: VSSQ termination.
2. DOUT *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRC needs to be satisfied prior to issuing a subsequent per-bank REFRESH command.

2.5 ZQ Calibration

The MPC command is used to initiate ZQ calibration, which calibrates the output driver impedance and CA/DQ ODT impedance across process, temperature, and voltage. ZQ calibration occurs in the background of device operation and is designed to eliminate any need for coordination between chan- nels (that is, it allows for channel independence). ZQ calibration is required each time that the PU-Cal value (MR3-OP[0]) is changed. Additional ZQ CALIBRATION commands may be required as the voltage and temperature change in the system environment. CA ODT values (MR11-OP[6:4]) and DQ ODT values (MR11-OP[2:0]) may be changed without performing ZQ calibration, as long as the PU-Cal value doesn't change.

There are two ZQ calibration modes initiated with the MPC command: ZQCAL START and ZQCAL LATCH. ZQCAL START initiates the calibration procedure, and ZQCAL LATCH captures the result and loads it into the drivers.

A ZQCAL START command may be issued anytime the device is not in a power-down state. A ZQCAL LATCH command may be issued anytime outside of power-down after tZQCAL has expired and all DQ bus operations have completed. The CA bus must maintain a deselect state during tZQLAT to allow CA ODT calibration settings to be updated. The DQ calibration value will not be updated until ZQCAL LATCH is performed and tZQLAT has been met. The following mode register fields that modify I/O parameters cannot be changed following a ZQCAL START command and before tZQCAL has expired:

- PU-Cal (pull-up calibration VOH point)
- PDDS (pull-down drive strength and Rx termination)
- DQ ODT (DQ ODT value)
- CA ODT (CA ODT value)

3 AC &DC Operating Conditions and Interface Specification

3.1 Absolute Maximum Ratings

Table 16 - Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	–0.4	2.1	V	1
VDD2 supply voltage relative to VSS	VDD2	–0.4	1.5	V	1
VDDQ supply voltage relative to VSS	VDDQ	–0.4	1.5	V	1
Voltage on any ball relative to VSS	VIN, VOUT	–0.4	1.5	V	
Storage temperature	TSTG	–55	125	˚C	2

Notes: 1. For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.
2. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

3.2 AC and DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 17 -Recommended DC Operating Conditions

Symbol	Min	Typ	Max	DRAM	Unit	Notes
VDD1	1.7	1.8	1.95	Core 1 power	V	1, 2
VDD2	1.06	1.1	1.17	Core 2 power/Input buffer power	V	1, 2, 3
VDDQ	0.57	0.60	0.65	I/O buffer power	V	2, 3
Or VDDQ	1.06	1.1	1.17	I/O buffer power	V	2, 3

Notes: 1. VDD1 uses significantly less power than VDD2.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

Table 18- Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current	IL	–4	4	μA	1, 2

Notes: 1. For CK_t, CK_c, CKE, CS, CA, ODT_CA and RESET_n. Any input 0V ≤ VIN ≤ VDD2. All other pins not under test = 0V.
2. CA ODT is disabled for CK_t, CK_c, CS, and CA.

Table 19- Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output leakage current	Ioz	–5	5	μA	1, 2

Notes: 1. For DQ, DQS_t, DQS_c and DMI. Any I/O 0V ≤ VOUT≤ VDDQ.
2. I/Os status are disabled: High impedance and ODT off.

Table 20 - Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	TOPER	Note 4	85	˚C
Elevated		85	95	˚C
Automotive		95	105	˚C

Notes: 1. Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.

2. When using the device in the elevated temperature range, some derating may be required. See Mode Registers for vendor-specific derating.

3. Either the device case temperature rating or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the standard or elevated temperature range. For example, TCASE could be above +85˚C when the temperature sensor indicates a temperature of less than +85˚C.

4. Refer to operating temperature range on top page.

3.3 Voltage Level

3.3.1. Input Levels for CKE

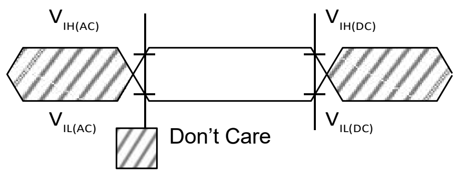
Table 21- Input Levels

Parameter	Symbol	Min	Max	Unit	Notes
Input HIGH level (AC)	VIH(AC)	0.75 × VDD2	VDD2 + 0.2	V	1
Input LOW level (AC)	VIL(AC)	–0.2	0.25 × VDD2	V	1
Input HIGH level (DC)	VIH(DC)	0.65 × VDD2	VDD2 + 0.2	V	
Input LOW level (DC)	VIL(DC)	–0.2	0.35 × VDD2	V	

Notes: 1. See the AC Overshoot and Undershoot section.

Figure 11-Input Timing Definition for CKE

Input level



3.3.2. Input Levels for RESET_n

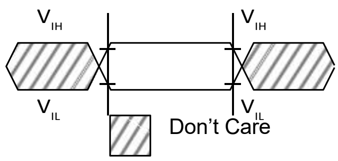
Table 22- Input Levels

Parameter	Symbol	Min	Max	Unit	Notes
Input HIGH level	VIH	0.80 × VDD2	VDD2 + 0.2	V	1
Input LOW level	VIL	–0.2	0.20 × VDD2	V	1

Note: 1. See the AC Overshoot and Undershoot section.

Figure 11-Input Timing Definition for RESET_n

Input level



3.3.3. Differential Input Voltage for CK

The minimum input voltage needs to satisfy both Vindiff_CK and Vindiff_CK/2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak-to-peak voltage centered on 0 volts differential and Vindiff_CK/2 is maximum and minimum peak voltage from 0 volts.

Figure 12-CK Differential Input Voltage

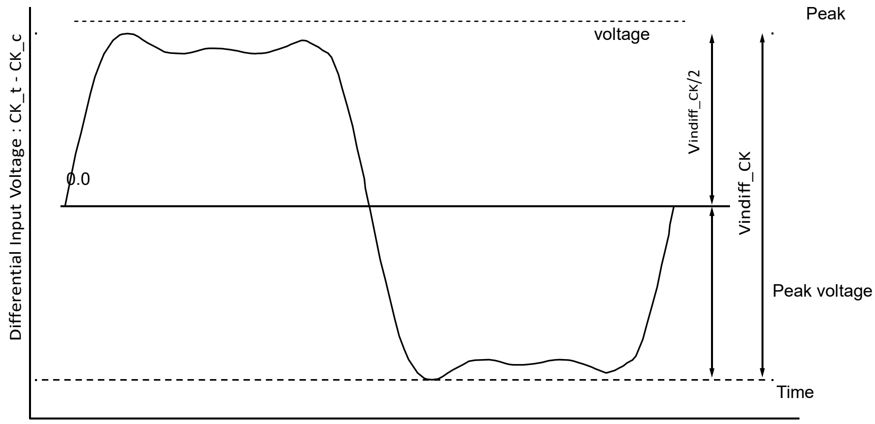


Table 23- CK Differential Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit	Note
		Min	Max	Min	Max	Min	Max		
CK differential input voltage	Vindiff_CK	420	–	380	–	360	–	mV	1

Note: 1. The peak voltage of differential CK signals is calculated in a following equation.

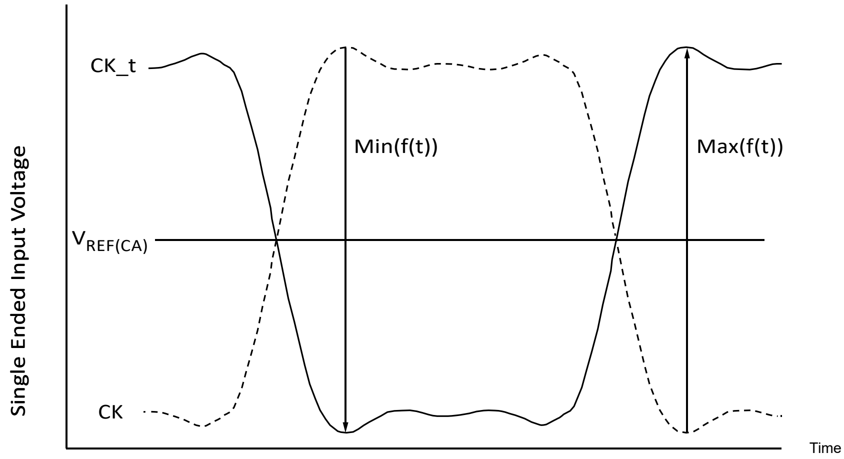
- Vindiff_CK = (Maximum peak voltage) - (Minimum peak voltage)
- Maximum peak voltage = MAX(f(t))
- Minimum peak voltage = MIN(f(t))
- f(t) = VCK_t - VCK_c

3.3.4. Peak Voltage Calculation Method

The peak voltage of differential clock signals are calculated in a following equation.

- VIH.DIFF.peak voltage = MAX(f(t))
- VIL.DIFF.peak voltage = MIN(f(t))
- f(t) = VCK_t - VCK_c

Figure 13-Definition of Differential Clock Peak Voltage

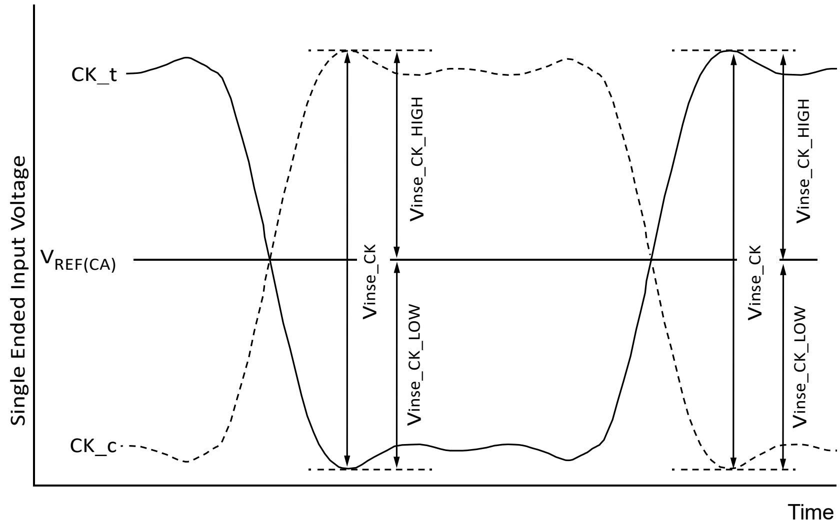


Note:1. VREF(CA) is device internal setting value by VREF training.

3.3.5. Single-Ended Input Voltage for Clock

The minimum input voltage needs to satisfy Vinse_CK, Vinse_CK_HIGH, and Vinse_CK_LOW specification at input receiver.

Figure 14-Clock Single-Ended Input Voltage



Note: 1. VREF(CA) is device internal setting value by VREF training.

Table 24- Clock Single-Ended Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Clock single-ended input voltage	Vinse_CK	210	–	190	–	180	–	mV

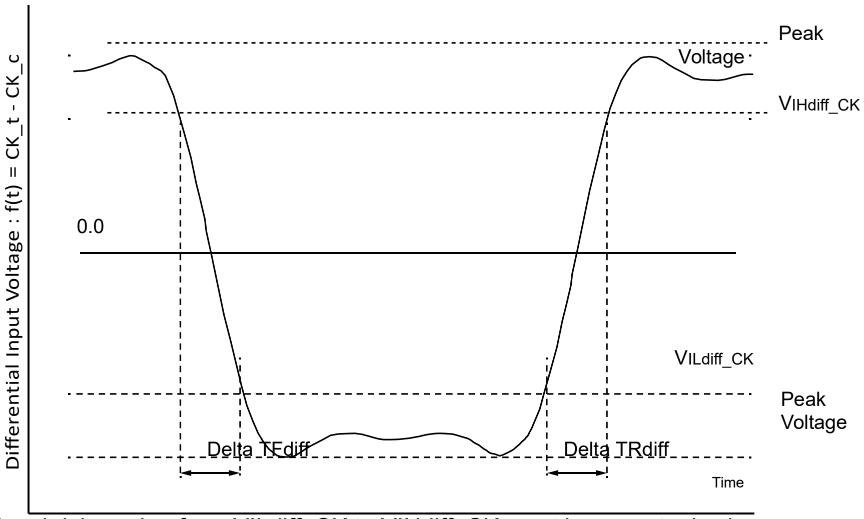
Table 25: Clock Single-Ended Input Voltage (Continued)

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Clock single-ended input voltage HIGH from VREF(CA)	Vinse_CK_HIGH	105	–	95	–	90	–	mV
Clock single-ended input voltage LOW from VREF(CA)	Vinse_CK_LOW	105	–	95	–	90	–	mV

3.3.6. Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below in figure and the tables.

Figure 15-Differential Input Slew Rate Definition for CK_t, CK_c



Notes: 1. Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.

Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

Table 26- Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t - CK_c)	VILdiff_CK	VIHdiff_CK	|VILdiff_CK - VIHdiff_CK|/ΔTRdiff
Differential input slew rate for falling edge (CK_t - CK_c)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK - VIHdiff_CK|/ΔTFdiff

Table 27-Differential Input Level for CK_t, CK_c

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Differential Input HIGH	VIHdiff_CK	175	–	155	–	145	–	mV
Differential Input LOW	VILdiff_CK	–	–175	–	–155	–	–145	mV

Table 28-Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Differential input slew rate for clock	SRIdiff_CK	2	14	2	14	2	14	V/ns

3.3.7. Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (CK_t, CK_c) must meet the requirements in table below. The differential input cross-point voltage VIX is measured from the actual cross-point of true and complement signals to the midlevel.

Figure 16-VixDefinition (Clock)

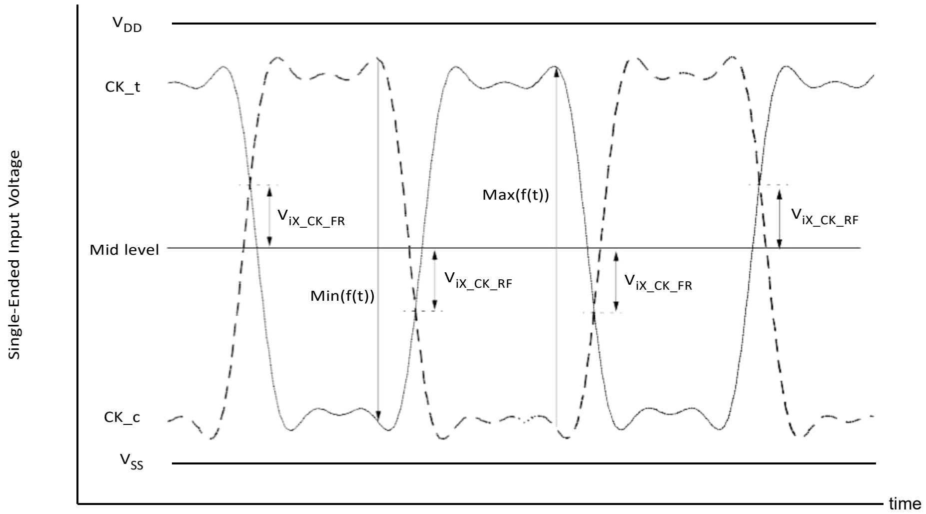


Table 29-Cross-Point Voltage for Differential Input Signals (Clock)

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Clock differential input cross-point voltage ratio	Vix_CK_ratio	–	25	–	25	–	25	%

Notes: 1. Vix_CK_ratio is defined by this equation: Vix_CK_ratio = Vix_CK_FR/|MIN(f(t))|
2. Vix_CK_ratio is defined by this equation: Vix_CK_ratio = Vix_CK_RF/MAX(f(t))
3. Vix_CK_FR is defined as delta between crosspoint (CK_t fall, CK_c rise) to MIN(f(t))/2.
4. In LPDDR4/4X un-terminated case, CK mid level is calculated as:
5. High level = VDDQ; Low level = VSS; Mid level = VDDQ/2
6. In LPDDR4/4X un-terminated case, mid level must be equal or lower than 369mV (33.6% of VDD2).
7. Notes 1–5 apply to entire table.

3.3.8. Differential Input Voltage for DQS

The minimum input voltage needs to satisfy both Vindiff_DQS and Vindiff_DQS/2 specification at input receiver and their measurement period is 1UI (tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS/2 is maximum and minimum peak voltage from 0 volts.

Figure 17-DQS Differential Input Voltage

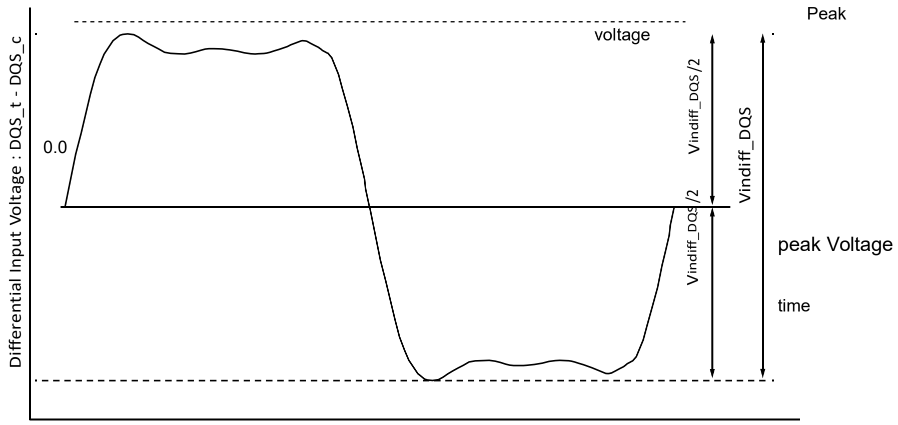


Table 30-DQS Differential Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit	Note
		Min	Max	Min	Max	Min	Max		
DQS differential input volt- age	Vindiff_DQS	360	–	360	–	340	–	mV	1

Notes: 1. The peak voltage of differential DQS signals is calculated in a following equation.

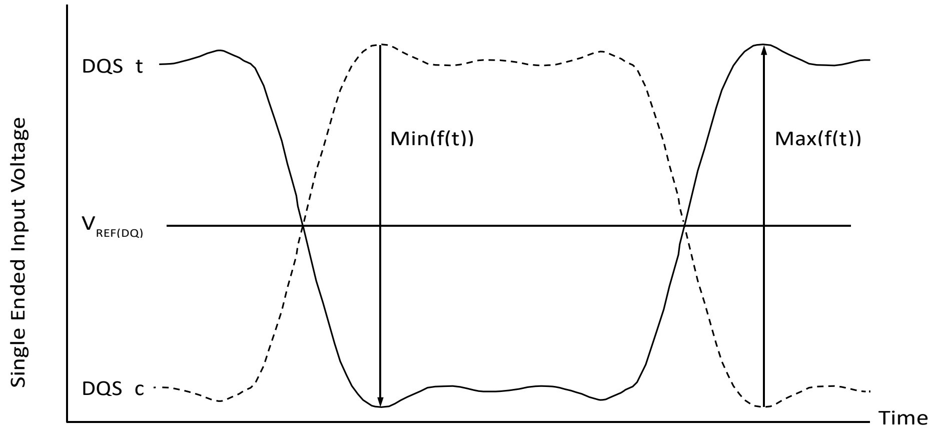
- Vindiff_DQS = (Maximum peak voltage) - (Minimum peak voltage)
- Maximum peak voltage = MAX(f(t))
- Minimum peak voltage = MIN(f(t))
- f(t) = VDQS_t - VDQS_c

3.3.9. Peak Voltage Calculation Method

The peak voltage of differential DQS signals are calculated in a following equation.

- VIH.DIFF.peakvoltage = MAX(f(t))
- VIL.DIFF.peak voltage = MIN(f(t))
- f(t) = VDQS_t - VDQS_c

Figure 18- Definition of Differential DQS Peak Voltage

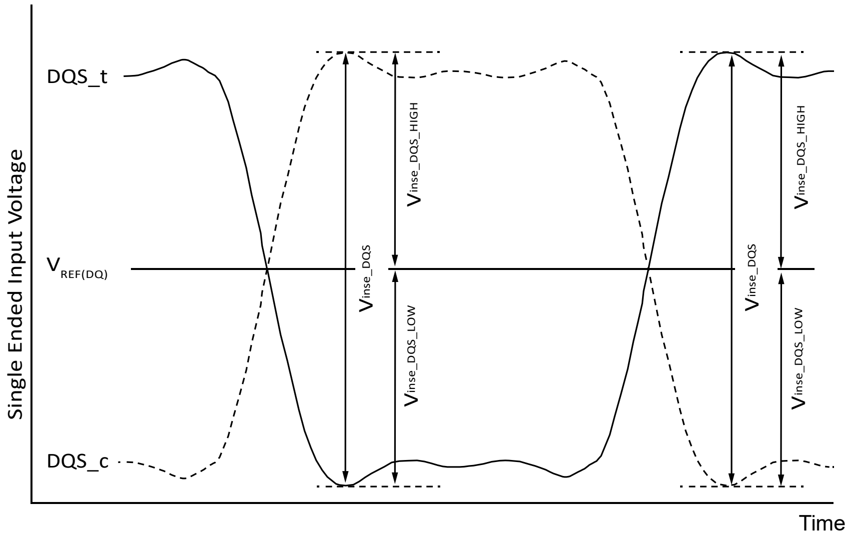


Note: 1. VREF(DQ) is device internal setting value by VREF training

3.3.10. Single-Ended Input Voltage

The minimum input voltage needs to satisfy Vinse_DQS, Vinse_DQS_HIGH, and Vinse_DQS_LOW specification at input receiver.

Figure 19-DQS Single-Ended Input Voltage



Note: 1. VREF(DQ) is device internal setting value by VREF training.

Table 31- DQS Single-Ended Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
DQS single-ended input voltage	V_{inse_DQS}	180	–	180	–	170	–	mV

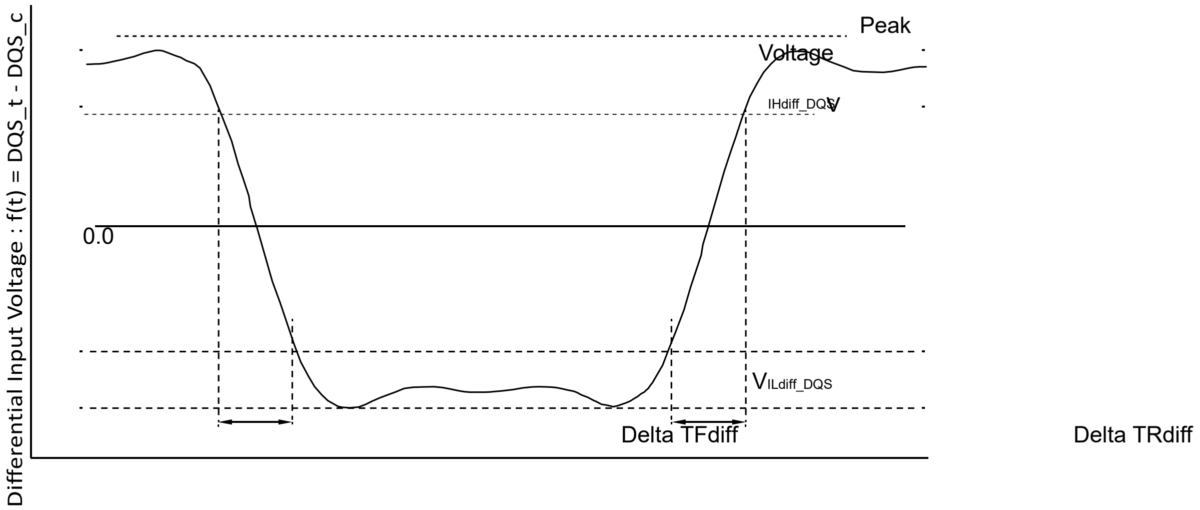
Table 30 -DQS Single-Ended Input Voltage (Continued)

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
DQS single-ended input voltage HIGH from VREF(DQ)	Vinse_DQS_HIGH	90	–	90	–	85	–	mV
DQS single-ended input voltage LOW from VREF(DQ)	Vinse_DQS_LOW	90	–	90	–	85	–	mV

3.3.11. Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown below in figure and the tables.

Figure 20-Differential Input Slew Rate Definition for DQS_t, DQS_c



Notes: 1. Differential signal rising edge from VILdiff_DQS to VIHdiff_DQS must be monotonic slope.
2. Differential signal falling edge from VIHdiff_DQS to VILdiff_DQS must be monotonic slope

Table 32-Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILdiff_DQS	VIHdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/ΔTRdiff
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHdiff_DQS	VILdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/ΔTFdiff

Table 33-Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Differential Input HIGH	VIHdiff_DQS	140	–	140	–	120	–	mV
Differential Input LOW	VILdiff_DQS	–	–140	–	–140	–	–120	mV

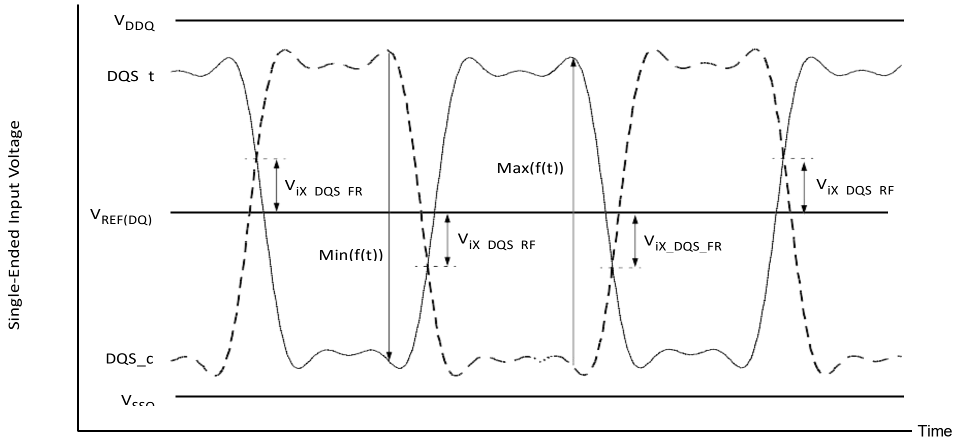
Table 34 Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Differential input slew rate	SRIdiff	2	14	2	14	2	14	V/ns

3.3.12. Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in table below. The differential input cross-point voltage VIX is measured from the actual cross-point of true and complement signals to the midlevel that is VREF(DQ).

Figure 21- VixDefinition (DQS)



Note: The base levels of Vix_DQS_FR and Vix_DQS_RF are VREF(DQ) that is device internal setting value by VREF training.

Table 35- Cross-Point Voltage for Differential Input Signals (DQS)

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
DQS differential input cross-point voltage ratio	Vix_DQS_ratio	–	20	–	20	–	20	%

Notes: 1. Vix_DQS_ratio is defined by this equation: Vix_DQS_ratio = Vix_DQS_FR/|MIN(f(t))|
2. Vix_DQS_ratio is defined by this equation: Vix_DQS_ratio = Vix_DQS_RF/MAX(f(t))
3. Notes 1 and 2 apply to entire table.

3.3.13. Input Levels for ODT_CA

Table 36-Input Levels for ODT_CA

Parameter	Symbol	Min	Max	Unit
ODT input HIGH level	VIHODT	0.75 × VDD2	VDD2 + 0.2	V
ODT input LOW level	VILODT	–0.2	0.25 × VDD2	V

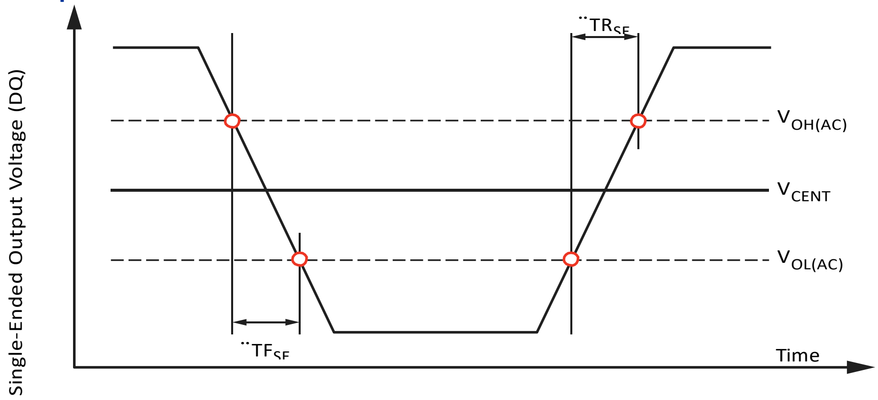
3.3.14. Single-Ended Output Slew Rate

Table 37- Single-Ended Output Slew Rate

Parameter	Symbol	Value		
		Min	Max	Units
Single-ended output slew rate (VOH = VDDQ x 0.5)	SRQse	3.0	9.0	V/ns
Output slew rate matching ratio (rise to fall)	–	0.8	1.2	–

Notes: 1. SR = Slew rate; Q = Query output; se = Single-ended signal.
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between VOL(AC) = 0.2 × VOH(DC) and VOH(AC) = 0.8 × VOH(DC).
5. Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.
6. Notes 1–5 apply to entire table.

Figure 22-Single-Ended Output Slew Rate Definition



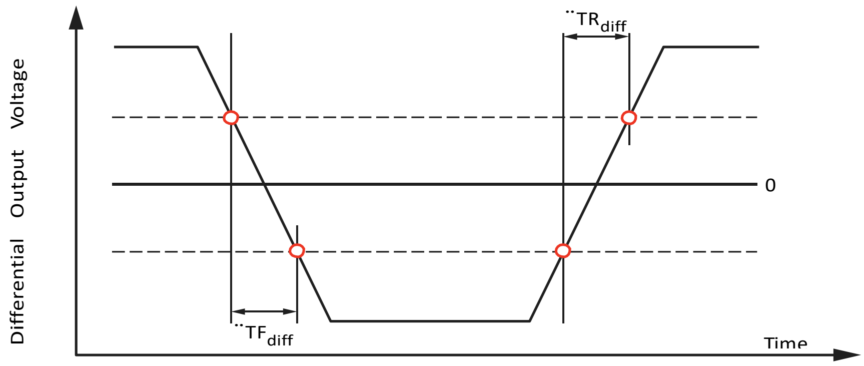
3.3.15. Differential Output Slew Rate

Table 38-Differential Output Slew Rate

Parameter	Symbol	Value		
		Min	Max	Units
Differential output slew rate (VOH = VDDQ x 0.5)	SRQdiff	6	18	V/ns

Notes: 1. SR = Slew rate; Q = Query output; se = Differential signal.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) = –0.8 × VOH(DC) and VOH(AC) = 0.8 × VOH(DC).
4. Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.
5. Notes 1–4 apply to entire table.

Figure 23-Differential Output Slew Rate Definition



3.3.16. Overshoot and Undershoot Specifications

Table 39-AC Overshoot/Undershoot Specifications

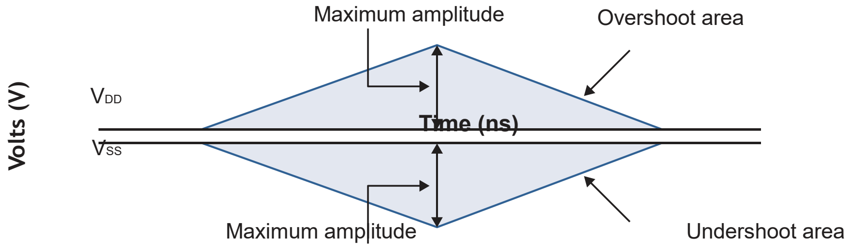
Parameter		1600	1866	3200	3733	4267	Unit
Maximum peak amplitude provided for overshoot area	MAX	0.3	0.3	0.3	0.3	0.3	V
Maximum peak amplitude provided for undershoot area	MAX	0.3	0.3	0.3	0.3	0.3	V
Maximum area above VDD/ VDDQ	MAX	0.1	0.1	0.1	0.1	0.1	V/ns
Maximum area below VSS/ VSSQ	MAX	0.1	0.1	0.1	0.1	0.1	V/ns

Notes: 1. VDD stands for VDD2 for CA[5:0], CK_t, CS_n, CKE, and ODT. VDD stands for VDDQ for DQ, DMI, DQS_t, and DQS_c.
2. VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE, and ODT. VSS stands for VSSQ for DQ, DMI, DQS_t, and DQS_c.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum VDD and VSS values.

Table 40-Overshoot/Undershoot Specification for CKE and RESET

Parameter	Specification
Maximum peak amplitude provided for overshoot area	0.35V
Maximum peak amplitude provided for undershoot area	0.35V
Maximum area above VDD	0.8 V-ns
Maximum area below VSS	0.8 V-ns

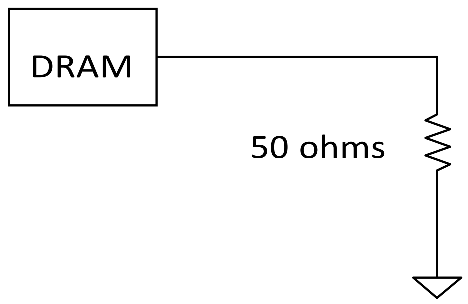
Figure 24-Overshoot and Undershoot Definition



3.3.17. Driver Output Timing Reference Load

Timing reference loads are not intended as a precise representation of any particular system environment or depiction of an actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 25- Driver Output Timing Reference Load

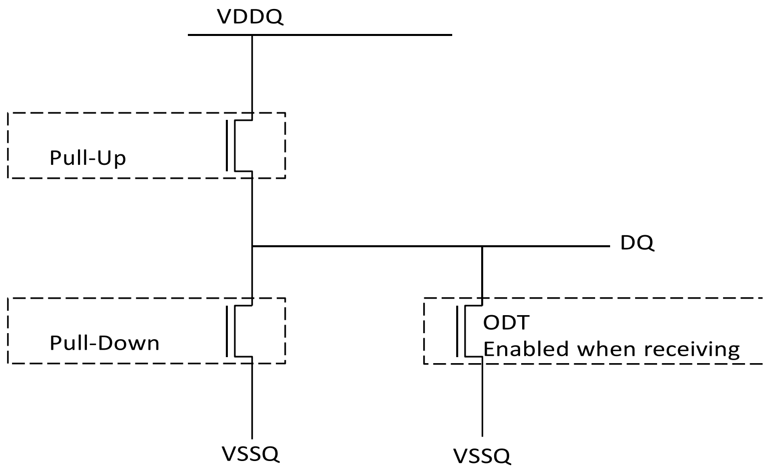


Note: 1. All output timing parameter values are reported with respect to this reference load; this reference load is also used to report slew rate.

3.3.18. LVSTL I/O System

LVSTL I/O cells are comprised of a driver pull-up and pull-down and a terminator.

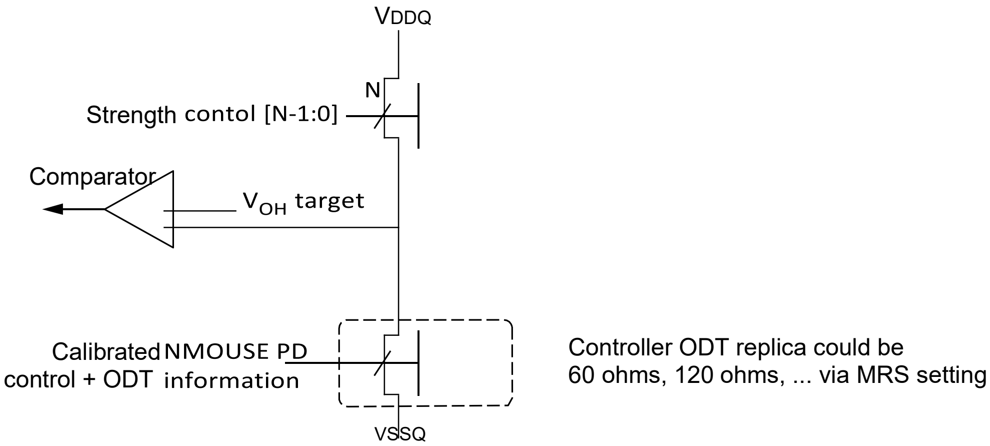
Figure 26-LVSTL I/O Cell



To ensure that the target impedance is achieved, calibrate the LVSTL I/O cell as following example:

1. Calibrate the pull-down device against a 240 ohm resistor to VDDQ via the ZQ pin.
   - Set strength control to minimum setting
   - Increase drive strength until comparator detects data bit is less than VDDQ/2
   - NMOS pull-down device is calibrated to 240 ohms
2. Calibrate the pull-up device against the calibrated pull-down device.
   - Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS)
   - Set strength control to minimum setting
   - Increase drive strength until comparator detects data bit is greater than VOH target
   - NMOS pull-up device is calibrated to VOH target

Figure 27- Pull-Up Calibration



3.3.19. Input/Output Capacitance

Table 41- Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance, CK_t and CK_c	C_{CK}	0.5	0.9	pF	
Input capacitance delta, CK_t and CK_c	C_{DCK}	0	0.09		3
Input capacitance, all other input-only pins	C_I	0.5	0.9		4
Input capacitance delta, all other input-only pins	C_{DI}	–0.1	0.1		5
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	C_{IO}	0.7	1.3		6
Input/output capacitance delta, DQS_t, DQS_c	C_{DDQS}	0	0.1		7
Input/output capacitance delta, DQ, DMI	C_{DIO}	–0.1	0.1		8
Input/output capacitance, ZQ pin	C_{ZQ}	0	5.0		

Notes: 1. This parameter applies to LPDDR4/LPDDR4x die only (does not include package capacitance).
2. This parameter is not subject to production testing; It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with VDD1, VDD2, VDDQ, and VSS applied; All other pins are left floating.
3. Absolute value of CCK_t – CCK_c.
4. CI applies to CS, CKE, and CA[5:0].
5. CDI = CI – 0.5 × (CCK_t + CCK_c); It does not apply to CKE.
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. CDIO = CIO – Average (CDQn, CDMI, CDQS_t, CDQS_c) in byte-lane.
9. Notes 1 and 2 apply to entire table.

4 Electrical Specifications

I_{DD} Parameters

Refer to IDD Specification Parameters and Test Conditions section for detailed conditions.

Table 42: LPDDR4X IDD Parameters – Single Die x32 Mode (16Gb Dual-Channel Die)

Symbol	Supply	Tc/4266Mb/s		Unit	Note
		95°C	105°C		
IDD01	VDD1	8.4	8.8	mA	
IDD02	VDD2	59.00	60.00		
IDD0Q	VDDQ	1.50	1.50		
IDD2P1	VDD1	2.4	2.4	mA	
IDD2P2	VDD2	5.4	7.2		
IDD2PQ	VDDQ	1.5	1.5		
IDD2PS1	VDD1	2.4	2.4	mA	
IDD2PS2	VDD2	5.4	7.2		
IDD2PSQ	VDDQ	1.5	1.5		
IDD2N1	VDD1	2.4	2.4	mA	
IDD2N2	VDD2	33	35		
IDD2NQ	VDDQ	1.5	1.5		
IDD2NS1	VDD1	2.4	2.4	mA	
IDD2NS2	VDD2	25	29		
IDD2NSQ	VDDQ	1.5	1.5		
IDD3P1	VDD1	2.4	2.4	mA	
IDD3P2	VDD2	9.8	10.00		
IDD3PQ	VDDQ	1.5	1.5		
IDD3PS1	VDD1	2.4	2.4	mA	
IDD3PS2	VDD2	9.8	10.00		
IDD3PSQ	VDDQ	1.5	1.5		
IDD3N1	VDD1	3.4	3.4	mA	
IDD3N2	VDD2	44	46		
IDD3NQ	VDDQ	1.5	1.5		
IDD3NS1	VDD1	3.4	3.4	mA	
IDD3NS2	VDD2	36	41		
IDD3NSQ	VDDQ	1.5	1.5		
IDD4R1	VDD1	15	15	mA	2, 3
IDD4R2	VDD2	400	400		
IDD4RQ	VDDQ	126.10	126.10		

Table 41- LPDDR4X IDD Parameters – Single Die x32 mode (16Gb Dual-Channel Die)

Symbol	Supply	Tc/4266Mb/s		Unit	Note
		95°C	105°C		
IDD4W1	VDD1	15	15	mA	2
IDD4W2	VDD2	300	300		
IDD4WQ	VDDQ	1.5	1.5		
IDD51	VDD1	35	35	mA	
IDD52	VDD2	195	200		
IDD5Q	VDDQ	1.50	1.50		
IDD5AB1	VDD1	7.8	8.0	mA	
IDD5AB2	VDD2	41	45		
IDD5ABQ	VDDQ	1.5	1.5		
IDD5PB1	VDD1	6.7	7	mA	
IDD5PB2	VDD2	41.00	45.00		
IDD5PBQ	VDDQ	1.50	1.50		

Notes: 1. Published IDD values except IDD4RQ are the maximum IDD values considering the worst-case conditions of process, temperature, and voltage.
2. BL = 16, DBI disabled.
3. IDD4RQ value is reference only. Typical value. VOH = 0.5 × VDDQ; TC = 25°C
4. VDD2= 1.06–1.17V; VDDQ = 0.57–0.65V; VDD1 = 1.70–1.95V;

Table 43-IDD6 Full-Array Self Refresh Current – Single Die x32 Mode (16Gb Dual-Channel Die)

Temperature	Supply	Full-Array Self Refresh Current	Unit
25°C	VDD1	0.65	mA
	VDD2	1.33	
	VDDQ	0.02	
95°C	VDD1	6.50	mA
	VDD2	18.00	
	VDDQ	1.50	
105°C	VDD1	8.00	mA
	VDD2	23.00	
	VDDQ	1.50	

Notes: 1. IDD6 25°C is the typical value in the distribution with nominal VDD and a reference-only value. IDD6 95°C, IDD6 105°C is the maximum IDD guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. When TC >105°C, self-refresh mode is not available.
3. IDD values reflect dual-channel operation with the same pattern for each channel.
4. VDD2= 1.06–1.17V; VDDQ = 0.57–0.65V; VDD1 = 1.70–1.95V

IDD Parameters

Refer to IDD Specification Parameters and Test Conditions section for detailed conditions.

Table 44- LPDDR4 IDD Parameters – Single Die x32 Mode (16Gb Dual-Channel Die)

Symbol	Supply	Tc/4266 Mb/s		Unit	Note
		95°C	105°C		
IDD01	VDD1	8.4	8.8	mA	
IDD02	VDD2	59	60		
IDD0Q	VDDQ	1.5	1.5		
IDD2P1	VDD1	2.4	2.4	mA	
IDD2P2	VDD2	5.4	7.2		
IDD2PQ	VDDQ	1.5	1.5		
IDD2PS1	VDD1	2.4	2.4	mA	
IDD2PS2	VDD2	5.4	7.2		
IDD2PSQ	VDDQ	1.5	1.5		
IDD2N1	VDD1	2.4	2.4	mA	
IDD2N2	VDD2	33.00	35.00		
IDD2NQ	VDDQ	1.50	1.50		
IDD2NS1	VDD1	2.40	2.40	mA	
IDD2NS2	VDD2	25.00	29.00		
IDD2NSQ	VDDQ	1.50	1.50		
IDD3P1	VDD1	2.40	2.40	mA	
IDD3P2	VDD2	9.80	10.00		
IDD3PQ	VDDQ	1.50	1.50		
IDD3PS1	VDD1	2.40	2.40	mA	
IDD3PS2	VDD2	9.80	10.00		
IDD3PSQ	VDDQ	1.50	1.50		
IDD3N1	VDD1	3.40	3.40	mA	
IDD3N2	VDD2	44.00	46.00		
IDD3NQ	VDDQ	1.50	1.50		
IDD3NS1	VDD1	3.40	3.40	mA	
IDD3NS2	VDD2	36.00	41.00		
IDD3NSQ	VDDQ	1.50	1.50		
IDD4R1	VDD1	15.00	15.00	mA	2, 3
IDD4R2	VDD2	300.00	300.00		
IDD4RQ	VDDQ	187.80	187.80		

Table 43- LPDDR4 IDD Parameters – Single Die x16 Mode (16Gb Single-Channel Die)

Symbol	Supply	Tc/4266Mb/s 95°C	Tc/4266Mb/s 105°C	Unit	Note
IDD4W1	VDD1	15.00	15.00	mA	2
IDD4W2	VDD2	300.00	300.00		
IDD4WQ	VDDQ	1.50	1.50		
IDD51	VDD1	35.00	35.00	mA	
IDD52	VDD2	195.00	200.00		
IDD5Q	VDDQ	1.50	1.50		
IDD5AB1	VDD1	7.80	8.00	mA	
IDD5AB2	VDD2	41.00	45.00		
IDD5ABQ	VDDQ	1.50	1.50		
IDD5PB1	VDD1	6.70	7.00	mA	
IDD5PB2	VDD2	41.00	45.00		
IDD5PBQ	VDDQ	1.50	1.50		

Notes: 1. Published IDD values except IDD4RQ are the maximum IDD values considering the worst-case conditions of process, temperature, and voltage.
2. BL = 16, DBI disabled.
3. IDD4RQ value is reference only. Typical value. VOH = 0.5 × VDDQ; TC = 25°C 4. VDD2= 1.06–1.17V; VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V;

Table 45- IDD6 Full-Array Self Refresh Current – Single Die x32 Mode (16Gb Dual-Channel Die)

Temperature	Supply	Full-Array Self Refresh Current	Unit
25°C	VDD1	0.65	mA
	VDD2	1.33	
	VDDQ	0.02	
95°C	VDD1	6.50	mA
	VDD2	18.00	
	VDDQ	1.50	
105°C	VDD1	8.00	mA
	VDD2	23.00	
	VDDQ	1.50	

Notes: 1. IDD6 25°C is the typical value in the distribution with nominal VDD and a reference-only value. IDD6 95°C, IDD6 105°C is the maximum IDD guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. When TC >105°C, self-refresh mode is not available.
3. IDD values reflect dual-channel operation with the same pattern for each channel.
4. VDD2= 1.06–1.17V; VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V;

List of Figures

List of Tables

Edition 2025-02
Published by
Xi'an UniIC Semiconductors Co., Ltd.

Xi'an: 4th Floor, Building A,
No. 38 Gaoxin 6th Road,
Xian High-tech Industries Development Zone
Xi'an, Shannxi 710075, P. R. China
Tel: +86-29-88318000
Fax: +86-29-88453299

info@unisemicon.com

Legal Disclaimer

THE INFORMATION GIVEN IN THIS INTERNET DATA SHEET SHALL IN NO EVENT BE REGARDED AS A GUARANTEE OF CONDITIONS OR CHARACTERISTICS. WITH RESPECT TO ANY EXAMPLES OR HINTS GIVEN HEREIN, ANY TYPICAL VALUES STATED HEREIN AND/OR ANY INFORMATION REGARDING THE APPLICATION OF THE DEVICE, UNIIC HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest UniIC Office.

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest UniIC Office.
UniIC Components may only be used in life-support devices or systems with the express written approval of UniIC, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

www.unisemicon.com