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1Gbit DDR3(L) SDRAM
EU RoHS Compliant Products

Data Sheet

Rev. E

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2022-09	A	Initial Release
2023-08	B	Add I grade Part Number，update IDD value
2023-09	C	Add 1866Mbps parameter
2023-11	D	Add the command truth table, power-up and MR description remove 667/800Mhz Update IDD value
2025-02	E	Add A2/A1 P/N in product list

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Contents

Contents....3
1 Overview....4
  1.1 Features....4
  1.2 Product List....5
  1.3 Input / Output Signal Functional Description....6
  1.4 Ball Configuration....8
  1.5 DDR3 SDRAM Addressing....9
2 Functional Description....10
  2.1 Command Truth Table....10
  2.2 Power-up Initialization Sequence....13
  2.3 Mode Register 0 (MR0)....14
  2.4 Mode Register 1 (MR1)....16
  2.5 Mode Register 2 (MR2)....18
  2.6 Mode Register 3 (MR3)....19
  2.7 Burst Order....20
  2.8 Refresh command....21
3 Operating Conditions and Interface Specification....22
  3.1 Absolute Maximum Ratings....22
  3.2 Operating Conditions....22
  3.3 Interface Test Conditions....23
  3.4 Voltage Levels....24
  3.5 Output Slew Rates....29
  3.6 ODT DC Impedance and Mid-Level Characteristics....29
  3.7 ODT DC Impedance Sensitivity on Temperature and Voltage Drifts....30
  3.8 Interface Capacitance....31
  3.9 Overshoot and Undershoot Specification....32
4 Electrical Specifications....34
5 Electrical Characteristics and Recommended A.C. Operating Conditions....38
6 Package Outlines....43
7 Product Type Nomenclature....44
List of Figures....45
List of Tables....46

1 Overview

1.1 Features

The 1Gbit DDR3(L) SDRAM offers the following key features:

- JEDEC Standard Compliant
- Power supplies: V_{DD} & V_{DDQ} = +1.35V (1.283V ~ 1.45V)
- Backward compatible to V_{DD} & V_{DDQ} = +1.5V ±0.075V
- Operating temperature range: (T_{CASE})
  - Commercial (0 °C to 95 °C)
  - Industrial, I (-40 °C to 95 °C)
  - Automotive2,A2(-40 °C to 105 °C)
  - Automotive1,A1(-40 °C to 125 °C)
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Fast clock rate: 933/1066MHz
- Differential Clock, CK & CK#
- Bidirectional differential data strobe
  - DQS & DQS#
- 8 internal banks for concurrent operation
- 8n-bit prefetch architecture
- Pipelined internal architecture
- Pipelined internal architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Additive Latency (AL): 0, CL-1, CL-2
- Programmable Burst lengths: 4, 8
- Burst type: Sequential / Interleave
- Output Driver Impedance Control
- Auto Refresh and Self Refresh
- Average refresh period
  - 8192 cycles/64ms (7.8us at 0°C $\leqq$ T_C $\leqq$ +85°C)
  - 8192 cycles/32ms (3.9us at +85°C < T_C $\leqq$ +95°C)
  - 8192 cycles/32ms (3.9us at +95°C < T_C $\leqq$ +105°C)
  - 8192 cycles/16ms (1.95us at +105°C < T_C $\leqq$ +125°C)
- Write Leveling
- ZQ Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- RoHS compliant
- 96-ball 7.5 x 13 x 1.0mm FBGA package
  - Pb and Halogen Free

1.2 Product List

Table 1 shows all possible products within the 1Gbit DDR3(L) SDRAM component generation.

Table 1 - Ordering Information for 1Gbit DDR3(L) Component

UniIC Part Number	Max. Clock frequency	CAS-RCD-RP latencies	Speed Sort Name	Package
1Gbit DDR3(L) SDRAM Components in x16 Organization				
Commercial Temperature Range (0 °C~ +95 °C)				
SCB13H1G160EF-11M	933 MHz	13-13-13	DDR3L–1866M	PG-FBGA-96
SCB13H1G160EF-09N	1066 MHz	14-14-14	DDR3L–2133N	PG-FBGA-96
Industrial Temperature Range (-40 °C~ +95 °C)				
SCB13H1G160EF-11MI	933 MHz	13-13-13	DDR3L–1866M	PG-FBGA-96
SCB13H1G160EF-09NI	1066 MHz	14-14-14	DDR3L–2133N	PG-FBGA-96
Automotive2 Temperature Range (-40 °C~ +105 °C)				
SCB13H1G160EF-11MA2	933 MHz	13-13-13	DDR3L–1866M	PG-FBGA-96
SCB13H1G160EF-09NA2	1066 MHz	14-14-14	DDR3L–2133N	PG-FBGA-96
Automotive1 Temperature Range (-40 °C~ +125 °C)				
SCB13H1G160EF-11MA1	933 MHz	13-13-13	DDR3L–1866M	PG-FBGA-96
SCB13H1G160EF-09NA1	1066 MHz	14-14-14	DDR3L–2133N	PG-FBGA-96

1.3 Input / Output Signal Functional Description

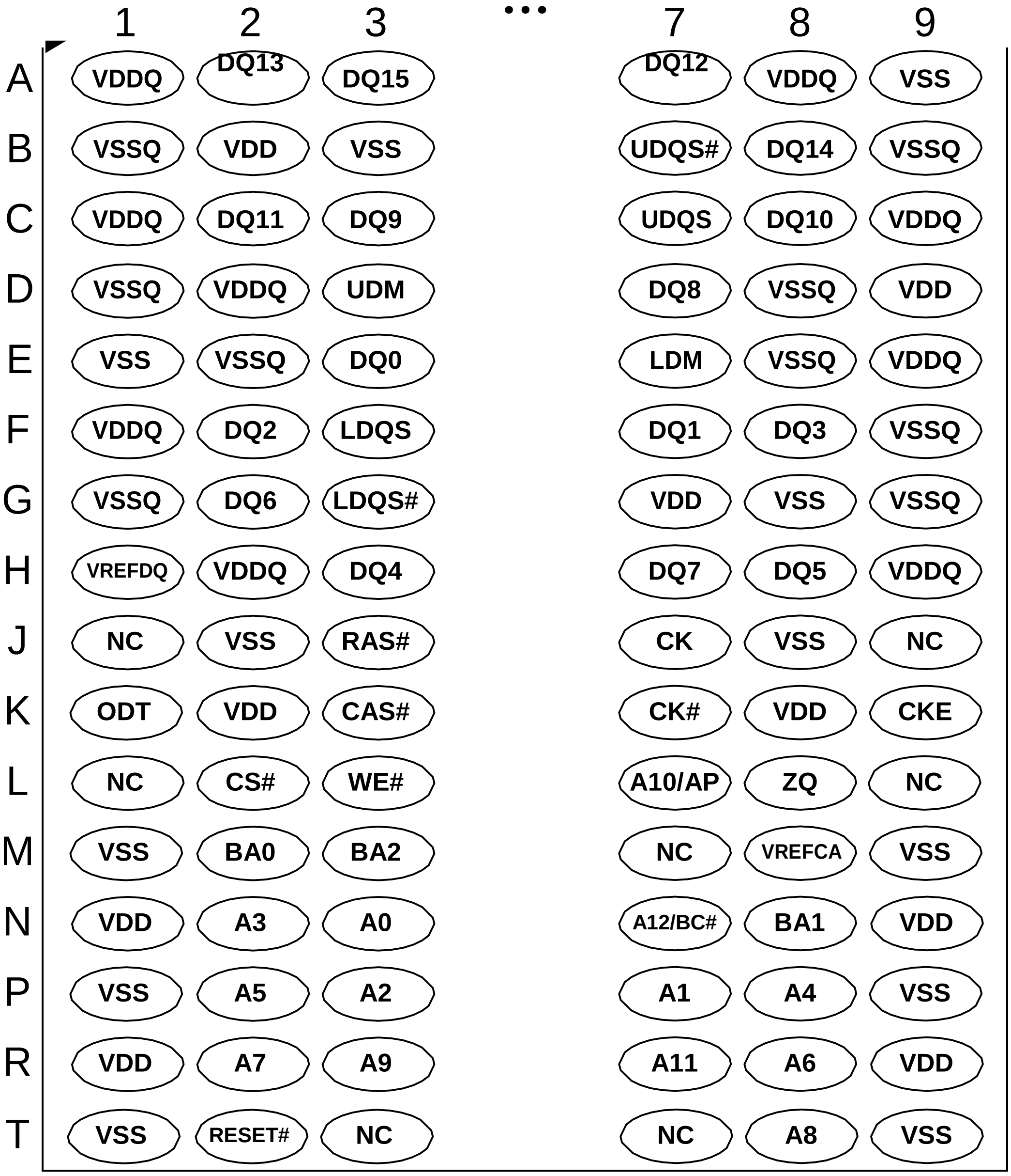
Table 2 - Input / Output Signal Functional Description

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK and CK# are driven by the system clock. All SDRAM input signals are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (Read) data is referenced to the crossings of CK and CK# (both directions of crossing).
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes LOW synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains LOW. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0-BA2	Input	**Bank Address:** BA0-BA2 define to which bank the BankActivate, Read, Write, or Bank Precharge command is being applied.
A0-A12	Input	**Address Inputs:** A0-A12 is sampled during row address (A0-A12) for Active commands and the column address (A0-A9) for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions). The address inputs also provide the op-code during Mode Register Set commands.
A10/AP	Input	**Auto-Precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH).
A12/BC#	Input	**Burst Chop:** A12/BC# is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH" either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH" the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW" the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# is held "HIGH" and CS# is asserted "LOW" the column access is started by asserting CAS# "LOW". Then, the Read or Write command is selected by asserting WE# “HIGH" or “LOW".
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, LDQS# UDQS UDQS#	Input / Output	**Bidirectional Data Strobe:** Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15. The data strobes LDOS and UDQS are paired with LDQS# and UDQS# to provide differential pair signaling to the system during both reads and writes.
LDM, UDM	Input	**Data Input Mask:** Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0-DQ15	Input / Output	**Data I/O:** The DQ0-DQ15 input and output data are synchronized with positive and negative edges of DQS and DQS#. The I/Os are byte-maskable during Writes.

Symbol	Type	Description
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3L SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS#. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.
RESET#	Input	**Active Low Asynchronous Reset:** Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
V_{DD}	Supply	**Power Supply:** +1.35V -0.067V/+0.1V. compatible to 1.5+/- 0.075V operation
V_{SS}	Supply	**Ground**
V_{DDQ}	Supply	**DQ Power:** +1.35V -0.067V/+0.1V. compatible to 1.5+/- 0.075V operation
V_{SSQ}	Supply	**DQ Ground**
V_{REFCA}	Supply	**Reference voltage for CA**
V_{REFDQ}	Supply	**Reference voltage for DQ**
ZQ	Supply	**Reference pin for ZQ calibration.**
NC	-	**No Connect:** These pins should be left unconnected.

1.4 Ball Configuration

Figure 1 - Ball out for 64 Mb ×16 Components (FBGA-96)



	1	2	3	• • •	7	8	9
A	VDDQ	DQ13	DQ15		DQ12	VDDQ	VSS
B	VSSQ	VDD	VSS		UDQS#	DQ14	VSSQ
C	VDDQ	DQ11	DQ9		UDQS	DQ10	VDDQ
D	VSSQ	VDDQ	UDM		DQ8	VSSQ	VDD
E	VSS	VSSQ	DQ0		LDM	VSSQ	VDDQ
F	VDDQ	DQ2	LDQS		DQ1	DQ3	VSSQ
G	VSSQ	DQ6	LDQS#		VDD	VSS	VSSQ
H	VREFDQ	VDDQ	DQ4		DQ7	DQ5	VDDQ
J	NC	VSS	RAS#		CK	VSS	NC
K	ODT	VDD	CAS#		CK#	VDD	CKE
L	NC	CS#	WE#		A10/AP	ZQ	NC
M	VSS	BA0	BA2		NC	VREFCA	VSS
N	VDD	A3	A0		A12/BC#	BA1	VDD
P	VSS	A5	A2		A1	A4	VSS
R	VDD	A7	A9		A11	A6	VDD
T	VSS	RESET#	NC		NC	A8	VSS

1.5 DDR3 SDRAM Addressing

Table 3 - 1Gbit DDR3 SDRAM Addressing

Configuration	64Mb × 16	Note
Number of Banks	8	
Bank Address	BA[2:0]	
Row Address	A[12:0]	
Column Address	A[9:0]	
Page Size	2KB	1)
Auto-Precharge	A10 | AP	
Burst length on-the-fly bit	A12 | BC#	

1) age size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per memory bank and calculated as follows: Page Size = $2^{COLBITS} \times ORG/8$, where COLBITS is the number of column address bits and ORG is the number of DQ bits for a given SDRAM configuration.

2 Functional Description

2.1 Command Truth Table

The truth table list the input signal values at a given clock edge which represent a command or state transition expected to be executed by the DDR3(L) SDRAM. **Table 4** lists all valid commands to the DDR3(L) SDRAM. For a detailed description of the various power mode entries and exits please refer to **Table 5**. In addition, the DM functionality is described in **Table 6**.

Table 4 - Command Truth Table

Function	Abbreviation	CKE		CS	RAS	CAS	WE	BA0 - BA2	A12 / BC	A10 / AP	A0 - A9,A11	Notes
		Previous Cycle	Current Cycle									
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code			
Refresh	REF	H	H	L	L	L	H	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	7)9)12)
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	7)8)9)12)
				L	H	H	H	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)			
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	10)
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	11)
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	6)12)
				H	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	6)12)
				H	X	X	X	X	X	X	X	

Notes 1) - 4) apply to the entire Command Truth Table.

Note 5) apply to all Read/Write command.

1) All DDR3(L) SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant.
2) RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3) Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4) "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5) Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS.
6) The Power Down Mode does not perform any refresh operations.
7) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8) Self refresh exit is asynchronous.
9) VREF(Both VREFDQ and VREFCA) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
10) The No Operation command (NOP) should be used in cases when the DDR3(L) SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3(L) SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11) The Deselect command performs the same function as a No Operation command.
12) Refer to the CKE Truth Table for more detail with CKE transition.

Table 5 - Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State 1)	CKE(N-1)2)	CKE(N)2)	Command (N)3) RAS#, CAS#, WE#, CS#	Action (N)3)	Note4)-7)
	Previous Cycle	Current Cycle			
Power Down	L	L	X	Maintain Power Down	8)9)
	L	H	DES or NOP	Power Down Exit	8)10)
Self Refresh	L	L	X	Maintain Self Refresh	9)11)
	L	H	DES or NOP	Self Refresh Exit	11)12)13)
Bank(s) Active	H	L	DES or NOP	Active Power Down Entry	8)10)14)
Reading	H	L	DES or NOP	Power Down Entry	8)10)14)15)
Writing	H	L	DES or NOP	Power Down Entry	8)10)14)15)
Precharging	H	L	DES or NOP	Power Down Entry	8)10)14)15)
Refreshing	H	L	DES or NOP	Precharge Power Down Entry	10)
All Banks Idle	H	L	DES or NOP	Precharge Power Down Entry	8)10)14)16)
	H	L	REF	Self Refresh Entry	14)16)17)
Any other state	Refer to **"Command Truth Table"** for more detail with all command signals				18)

1) Current state is defined as the state of the DDR3(L) SDRAM immediately prior to clock edge N.
2) CKE(N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
3) COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.
4) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6) CKE must be registered with the same value on $t_{CKE(MIN)}$ consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the $t_{CKE(MIN)}$ clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + t_{CKE(MIN)} + t_{IH}$.
7) DES and NOP are defined in **"Command Truth Table".**
8) The Power Down does not perform any refresh operations
9) X means Don't care (including floating around V_{REFCA}) in Self Refresh and Power Down. It also applies to address pins.
10) Valid commands for Power Down Entry and Exit are NOP and DES only

11) V_{REF} (both V_{REFCA} and V_{REFDQ}) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.

12) On Self Refresh Exit DES or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read, or ODT commands may be issued only after t_{XSDLL} is satisfied.

13) Valid commands for Self Refresh Exit are NOP and DES only.

14) Self Refresh can not be entered while Read or Write operations are in progress.

15) If all banks are closed at the conclusion of a read, write or precharge command then Precharge Power-down is entered, otherwise Active Power-down is entered.

16) 'Idle state' is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is High, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, $t_{ZQ.INIT}$, $t_{ZQ.OPER}$, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, t_{XPDLL}, etc.).

17) Self Refresh mode can only be entered from the All Banks Idle state.

18) Must be a legal command as defined in **"Command Truth Table"**

Table 6 - Data Mask (DM) Truth Table

Name (Function)	DM	DQs
Write Enable	L	Valid
Write Inhibit	H	X

2.2 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

OR

   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After RESET# is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3(L) SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=max (tXS ; 5 x tCK)
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3(L) SDRAM is now ready for normal operation.

2.3 Mode Register 0 (MR0)

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR (write recovery time for auto-precharge) and DLL control for precharge Power-Down, which includes various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting Low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to **Table 7.**

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0[1]	PPD	WR			DLL	TM	CL			RBT	CL	BL	

Table 7 - MR0 Mode register Definition (BA[2:0]=000$_B$)

Field	Bits[1]	Description
BL	A[1:0]	**Burst Length (BL) and Control Method** Number of sequential bits per DQ related to one Read/Write command. 00_B **BL8MRS** mode with fixed burst length of 8. A12 | BC# at Read or Write command time is Don't care at read or write command time.(default) 01_B **BLOTF** on-the-fly (OTF) enabled using A12 | BC# at Read or Write command time. When A12 | BC# is High during Read or Write command time a burst length of 8 is selected (BL8OTF mode). When A12 | BC# is Low, a burst chop of 4 is selected (BC4OTF mode). Auto-Precharge can be enabled or disabled. 10_B **BC4MRS** mode with fixed burst chop of 4 with $t_{CCD} = 4 \times n_{CK}$. A12 | BC# is Don't care at Read or Write command time. 11_B **BL8MRS**
RBT	A3	**Read Burst Type** 0_B Nibble Sequential(default) 1_B Interleaved
CL	A[6:4,2]	**CAS Latency (CL)** CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. 0010_B CL = 5 0100_B CL = 6 0110_B CL = 7 1000_B CL = 8 1010_B CL = 9(default) 1100_B CL = 10 1110_B CL = 11 0001_B CL = 12 0011_B CL = 13 0101_B CL = 14 0111_B CL = 15 1001_B CL = 16 Note: The CL is 9 for all other bit combinations
TM	A7	**Test Mode** The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in this table. Programming bit A7 to a 1 places the DDR3 SDRAM into a test mode that is only used by the SDRAM manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1. 0_B Normal Mode 1_B Vendor specific test mode

Field	Bits[1]	Description
DLLres	A8	**DLL Reset** The internal DLL Reset bit is self-clearing, meaning it returns back to the value of 0 after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, t_{DLLK} must be met before any functions that require the DLL can be used (i.e. Read commands or synchronous ODT operations). 0_B No DLL Reset 1_B DLL Reset triggered
WR	A[11:9]	**Write Recovery for Auto-Precharge** Number of clock cycles for write recovery during Auto-Precharge. WR_{MIN} in clock cycles is calculated by dividing $t_{WR(MIN)}$ (in ns) by the actual $t_{CK(AVG)}$ (in ns) and rounding up to the next integer: WR_{MIN} [n_{CK}] = Roundup($t_{WR(MIN)}$[ns] / $t_{CK.AVG}$[ns]). The WR value in the mode register must be programmed to be equal or larger than WR_{MIN}. 000_B WR=16 001_B WR=5 010_B WR=6 011_B WR=7 100_B WR=8 101_B WR=10 110_B WR=12 111_B WR=14
PPD	A12	**Precharge Power-Down DLL Control** Active Power-Down will always be with DLL-on. Bit A12 will have no effect in this case. For Precharge Power-Down, bit A12 in MR0 is used to select the DLL usage as shown below. 0_B **Slow Exit.** DLL is frozen during precharge Power-down.Read and synchronous ODT commands are only allowed after t_{XPDLL}. 1_B **Fast Exit.** DLL remains on during precharge Power-down.Any command can be applied after t_{XP}, provided that other timing parameters are satisfied.

[1] A13 - even if not available on a specific device - must be programmed to 0_B

2.4 Mode Register 1 (MR1)

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, R_{TT}_Nom impedance, additive latency (AL), Write leveling enable and Qoff (output disable). The Mode Register MR1 is written by asserting Low on CS#, RAS#, CAS#, WE#, High on BA0 and Low on BA1and BA2, while controlling the states of address pins according to **Table 8**.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0 1)	Qoff	0 1)	0 1)	RTT_nom	0 1)	Level	RTT_nom	DIC	AL		RTT_nom	DIC	DLL

Table 8 - MR1 Mode Register Definition (BA[2:0]=001$_B$)

Field	Bits 1)	Description
DLLdis	A0	**DLL Disable** The DLL must be enabled for normal operation. DLL enable is required during power up initialization, after reset and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is enabled, a DLL reset must be issued afterwards. Any time the DLL is reset, t_{DLLK} clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{DQSCK}, t_{AON}, t_{AOF} or t_{ADC} parameters. During t_{DLLK}, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. 0_B DLL is enabled 1_B DLL is disabled
DIC	A[5, 1]	**Output Driver Impedance Control** 00_B: Ron = 40 Ω = RZQ/6 01_B: Ron = 34 Ω =RQZ/7 (nominal 34.3 Ω, with nominal RZQ = 240 Ω) 10_B: Ron = 48 Ω = RZQ/5 11_B: Ron = 60 Ω = RZQ/4
R_{TT_NOM}	A[9, 6, 2]	**Nominal Termination Resistance of ODT** **Notes** *1. If R_{TT_NOM} is used during Writes, only the values $R_{ZQ}/2$, $R_{ZQ}/4$ and $R_{ZQ}/6$ are allowed.* *2. In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all R_{TT}_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only R_{TT_NOM} settings of $R_{ZQ}/2$, $R_{ZQ}/4$ and $R_{ZQ}/6$ are allowed.* *3. All other bit combinations are reserved.* 000_B ODT disabled, R_{TT_NOM} = off 001_B RTT60 = RZQ / 4 (nominal 60 Ω with nominal RZQ = 240 Ω) 010_B RTT120 = RZQ / 2 (nominal 120 Ω with nominal RZQ = 240 Ω 011_B RTT40 = RZQ / 6 (nominal 40 Ω with nominal RZQ = 240 Ω) 100_B RTT20 = RZQ / 12 (nominal 20 Ω with nominal RZQ = 240 Ω) 101_B RTT30 = RZQ / 8 (nominal 30 Ω with nominal RZQ = 240 Ω) Note: The RTT is 30 = RZQ/8 for all other bit combinations

Field	Bits[1]	Description
AL	A[4, 3]	**Additive Latency (AL)** Any read or write command is held for the time of Additive Latency (AL) before it is issued as internal read or write command. **Notes** *1. AL has a value of CL - 1 or CL - 2 as per the CL value programmed in the MR0 register.* 00_B AL = 0 (AL disabled) 01_B AL = CL - 1 10_B AL = CL - 2 11_B AL = 0
Write Leveling enable	A7	**Write Leveling Mode** 0_B **Write Leveling Mode** Disabled, Normal operation mode 1_B **Write Leveling Mode** Enabled
Qoff	A12	**Output Disable** Under normal operation, the SDRAM outputs are enabled during read operation and write leveling for driving data (Qoff bit in the MR1 is set to 0_B). When the Qoff bit is set to 1_B, the SDRAM outputs (DQ, DQS, DQS#) will be disabled - also during write leveling. Disabling the SDRAM outputs allows users to run write leveling on multiple ranks and to measure I_{DD} currents during Read operations, without including the output. 0_B Output buffer enabled 1_B Output buffer disabled

1) A8, A10-A11, A13 must be programmed to 0_B during MRS.

2.5 Mode Register 2 (MR2)

The Mode Register MR2 stores the data for controlling refresh related features, R_{TT_WR} impedance, and CAS write latency. The Mode Register MR2 is written by asserting Low on CS#, RAS#, CAS#, WE#, High on BA1 and Low on BA0 and BA2, while controlling the states of address signals according to **Table 9**.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0[1]	0[1]	0[1]	Rtt_WR		0[1]	SRT	ASR	CWL			PASR		

Table 9 - MR2 Mode Register Definition (BA[2:0]=010_B)

<table>
<tr><th>Field</th><th>Bits[1]</th><th>Description</th></tr>
<tr><td>PASR</td><td>A[2:0]</td><td>**Partial Array Self Refresh (PASR)**
If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified self refresh location may get lost if self refresh is entered. During non-self-refresh operation, data integrity will be maintained if t_{REFI} conditions are met.
000_B Full array (Banks 000_B - 111_B)
001_B Half Array(Banks 000_B - 011_B)
010_B Quarter Array(Banks 000_B - 001_B)
011_B 1/8th array (Banks 000_B)
100_B 3/4 array(Banks 010_B - 111_B)
101_B Half array(Banks 100_B - 111_B)
110_B Quarter array(Banks 110_B - 111_B)
111_B 1/8th array(Banks 111_B)</td></tr>
<tr><td>CWL</td><td>A[5:3]</td><td>**CAS Write Latency (CWL)**
Number of clock cycles from internal write command to first write data in.
000_B 5 ($t_{CK.AVG} \geq$ 2.5 ns)
001_B 6 (2.5 ns > $t_{CK.AVG} \geq$ 1.875 ns)
010_B 7 (1.875 ns > $t_{CK.AVG} \geq$ 1.5 ns)
011_B 8 (1.5 ns > $t_{CK.AVG} \geq$ 1.25 ns)
011_B 9 (1.25 ns > $t_{CK.AVG} \geq$ 1.07ns)
011_B 10 (1.07 ns > $t_{CK.AVG} \geq$ 0.935 ns)
011_B 11 (0.935 ns > $t_{CK.AVG} \geq$ 0.833 ns)
011_B 12 (0.833 ns > $t_{CK.AVG} \geq$ 0.75 ns)</td></tr>
<tr><td>ASR</td><td>A6</td><td>**Auto Self-Refresh (ASR)**
When enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values.
0_B Manual SR reference (SRT)
1_B ASR enable</td></tr>
<tr><td>SRT</td><td>A7</td><td>**Self-Refresh Temperature Range (SRT)**
The SRT bit must be programmed to indicate T_{OPER} >105°C during subsequent self refresh operation. The high temperature self refresh has to be enable by MR2 bit A7 & A11 & A12
0_B Normal operating temperature range
1_B Extended operating temperature range
<table>
<tr><th>Refresh period(ms)</th><th>MR2[7]</th><th>MR2[12]</th><th>MR2[11]</th></tr>
<tr><td>32</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>8</td><td>1</td><td>1</td><td>X</td></tr>
</table>
Note: When the High Temperature Self Refresh is enabled there is an increase of I_{DD6}</td></tr>
<tr><td>R_{TT_WR}</td><td>A[10:9]</td><td>**Dynamic ODT mode and R_{TT_WR} Pre-selection**
00_B Dynamic ODT mode disabled
01_B Dynamic ODT mode enabled with R_{TT_WR} = RZQ/4 = 60 Ω
10_B Dynamic ODT mode enabled with R_{TT_WR} = RZQ/2 = 120Ω
10_B Dynamic ODT mode enabled with R_{TT_WR} = RZQ/6 = 40Ω</td></tr>
</table>

1) A8, A11-A13 must be programmed to 0B during MRS.

2.6 Mode Register 3 (MR3)

The Mode Register MR3 controls Multipurpose registers and optional On-die thermal sensor (ODTS) feature. The Mode Register MR3 is written by asserting Low on CS#, RAS#, CAS#,WE#, High on BA1 and BA0, and Low on BA2 while controlling the states of address signals according to **Table 10**.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	MPR	MPR loc	

Table 10 - MR3 Mode Register Definition (BA[2:0]=011$_B$)

Field	Bits(1)	Description
MPR loc	A[1:0]	**Multi Purpose Register Location** 00_B Pre-defined data pattern for read synchronization 01_B RFU 10_B RFU 11_B RFU
MPR	A2	**Multi Purpose Register Enable** *Note: When MPR is disabled, MR3 A[1:0] will be ignored.* 0_B MPR disabled, normal memory operation 1_B Dataflow from the Multi Purpose register MPR

1) A13 - even if not available on a specific device - must be programmed to 0_B.

2.7 Burst Order

Accesses within a given burst may be interleaved or nibble sequential depending on the programmed bit A3 in the mode register MR0.

Regarding read commands, the lower 3 column address bits CA[2:0] at read command time determine the start address for the read burst.

Regarding write commands, the burst order is always fixed. For writes with a burst length of 8, the inputs on the lower 3 column address bits CA[2:0] are ignored during the write command. For writes with a burst being chopped to 4, the input on column address 2 (CA[2]) determines if the lower or upper four burst bits are selected. In this case, the inputs on the lower 2 column address bits CA[1:0] are ignored during the write command. The following table shows burst order versus burst start address for reads and writes of bursts of 8 as well as of bursts of 4 operation (burst chop).

Table 11 - Bit Order during Burst

Burst Length	Command	Column Address 2:0			Interleaved Burst Sequence								Nibble Sequential Burst Sequence								Note
					Bit Order within Burst								Bit Order within Burst								
		CA2	CA1	CA0	1.	2.	3.	4.	5.	6.	7.	8.	1.	2.	3.	4.	5.	6.	7.	8.	
8	READ	0	0	0	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	1)
		0	0	1	**1**	0	3	2	**5**	4	7	6	**1**	2	3	0	**5**	6	7	4	1)
		0	1	0	**2**	3	0	1	**6**	7	4	5	**2**	3	0	1	**6**	7	4	5	1)
		0	1	1	**3**	2	1	0	**7**	6	5	4	**3**	0	1	2	**7**	4	5	6	1)
		1	0	0	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	1)
		1	0	1	**5**	4	7	6	**1**	0	3	2	**5**	6	7	4	**1**	2	3	0	1)
		1	1	0	**6**	7	4	5	**2**	3	0	1	**6**	7	4	5	**2**	3	0	1	1)
		1	1	1	**7**	6	5	4	**3**	2	1	0	**7**	4	5	6	**3**	0	1	2	1)
	WRITE	V	V	V	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	1)2)
4 (Burst Chop Mode)	READ	0	0	0	**0**	1	2	3	**T**	T	T	T	**0**	1	2	3	**T**	T	T	T	1)3)4)
		0	0	1	**1**	0	3	2	**T**	T	T	T	**1**	2	3	0	**T**	T	T	T	1)3)4)
		0	1	0	**2**	3	0	1	**T**	T	T	T	**2**	3	0	1	**T**	T	T	T	1)3)4)
		0	1	1	**3**	2	1	0	**T**	T	T	T	**3**	0	1	2	**T**	T	T	T	1)3)4)
		1	0	0	**4**	5	6	7	**T**	T	T	T	**4**	5	6	7	**T**	T	T	T	1)3)4)
		1	0	1	**5**	4	7	6	**T**	T	T	T	**5**	6	7	4	**T**	T	T	T	1)3)4)
		1	1	0	**6**	7	4	5	**T**	T	T	T	**6**	7	4	5	**T**	T	T	T	1)3)4)
		1	1	1	**7**	6	5	4	**T**	T	T	T	**7**	4	5	6	**T**	T	T	T	1)3)4)
	WRITE	0	V	V	**0**	1	2	3	**X**	X	X	X	**0**	1	2	3	**X**	X	X	X	1)2)4)5)
		1	V	V	**4**	5	6	7	**X**	X	X	X	**4**	5	6	7	**X**	X	X	X	1)2)4)5)

1) 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

2) V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

3) T: output drivers for data and strobe are in high impedance.

4) In case of BC4MRS (burst length being fixed to 4 by MR0 setting), the internal write operation starts two clock cycles earlier than for the BL8 modes. This means that the starting point for t_{WR} and t_{WTR} will be pulled in by two clocks. In case of BC4OTF mode (burst length being selected on-the-fly via A12 | BC#), the internal write operation starts at the same point in time as a burst of 8 write operation. This means that during on-the-fly control, the starting point for t_{WR} and t_{WTR} will not be pulled in by two clocks.

5) X: Don’t Care.

2.8 Refresh command

A delay between the refresh command and next valid command, except NOP or DES, must be greater than or equal to the minimum refresh cycle time t_{RFC}(min), Note that the t_{RFC} timing paramenter depends on memory density.

In general, a refresh command needs to be issued to the DDR3(L) SDRAM regularly every t_{REFI} interval, the t_{REFI} I is effected by the operation temperature, the **Table 12** show the relationship between t_{REFI} and the component operation temperature.

Table 12 - The relationship between tREFI and component Operating Temperature

Parameter	T_{REFI}	Operating Temperature		Note[1)-3)]
		Min.	Max.	
Refresh interval	7.8us	-40°C	+85°C	Commercial Temperature
	3.9us	-40°C	+95°C	Industrial Temperature
	1.95us	-40°C	+105°C	Industrial plus Temperature

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported.
3) Above 105 ℃ the Auto-Refresh command interval has to be reduced to t_{REFI}= 1.95 µs.

3 Operating Conditions and Interface Specification

3.1 Absolute Maximum Ratings

Table 13 - Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage on V_{DD} ball relative to V_{SS}	V_{DD}	–0.4	+1.8	V	1)3)
Voltage on V_{DDQ} ball relative to V_{SS}	V_{DDQ}	–0.4	+1.8	V	1)3)
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	+1.8	V	1)
Storage Temperature	T_{STG}	–55	+100	°C	1)2)

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratingconditions for extended periods may affect reliability

2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3) VDD and VDDQ must be within 300 mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

3.2 Operating Conditions

Table 14 - DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.425	1.5	1.575	V	1)2)4)
		1.283	1.35	1.45	V	1)2)3)
Supply Voltage for Output	V_{DDQ}	1.425	1.5	1.575	V	1)2)4)
		1.283	1.35	1.45	V	1)2)3)
Reference Voltage for DQ, DM inputs	$V_{REFDQ(DC)}$	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	5)6)
Reference Voltage for ADD, CMD inputs	$V_{REFCA(DC)}$	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	5)6)
External Calibration Resistor connected from ZQ ball to ground	R_{ZQ}	237.6	240.0	242.4	Ω	7)

1) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together

2) Under all conditions V_{DDQ} must be less than or equal to V_{DD}.

3) If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.

4) Under these supply voltages, the device operates to this DDR3L specifcation

5) The ac peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF.DC}$ by more than ±1% V_{DD} (for reference: approx. ± 15 mV for DDR3).

6) For reference: approx. $V_{DD}/2 \pm 15$ mV for DDR3, approx. $V_{DD}/2 \pm 13.5$ mV for DDR3L

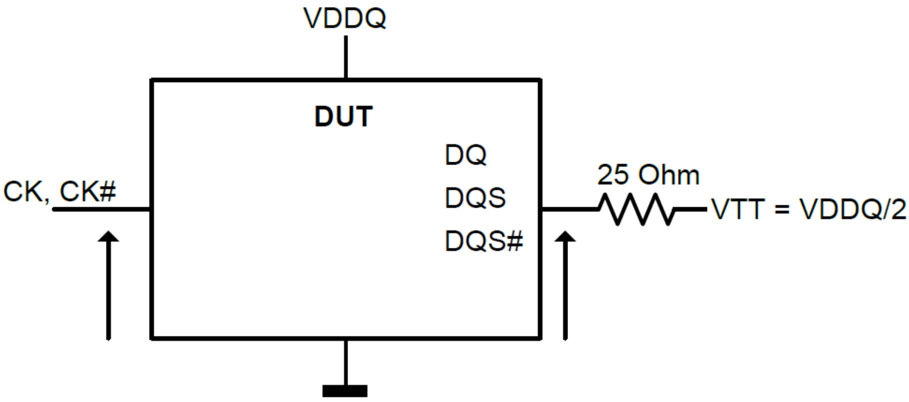
7) The external calibration resistor R_{ZQ} can be time-shared among DRAMs in multi-rank DIMMs.

3.3 Interface Test Conditions

错误!未找到引用源。 represents the effective reference load of 25 Ω used in defining the relevant timing parameters of the device as well as for output slew rate measurements. It is not intended as either a precise representation of the typical system environment nor a depiction of the actual load presented by a

Production tester System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 2 - Reference Load for AC Timings and Output Slew Rates



The Timing Reference Points are the idealized input and output nodes / terminals on the outside of the packaged SDRAM device as they would appear in a schematic or an IBIS model.

The output timing reference voltage level for single ended signals is the cross point with $V_{TT.}$

The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. DQS#) signal.

3.4 Voltage Levels

DC and AC Logic Input Levels

Single-Ended Signals

Table 15 shows the input levels for single-ended input signals.

Table 15 - DC and AC Input Levels for Single-Ended Command, Address and Control Signals

Parameter	Symbol	DDR3-1866,2133		Unit	Note
		Min.	Max.		
DC input logic high	$V_{IH.CA.DC100}$	V_{REF} + 0.100	V_{DD}	V	1)
DC input logic low	$V_{IL.CA.DC100}$	V_{SS}	V_{REF} - 0.100	V	1)
AC input logic high	$V_{IH.CA.AC175}$	-	-	V	1)
AC input logic low	$V_{IL.CA.AC175}$	-	-	V	1)
AC input logic high	$V_{IH.CA.AC150}$	-	-	V	1)
AC input logic low	$V_{IL.CA.AC150}$	-	-	V	1)
AC input logic high	$V_{IH.CA.AC135}$	V_{REF} + 0.135	See 2)	V	1)
AC input logic low	$V_{IL.CA.AC135}$	See 2)	V_{REF} - 0.135	V	1)
AC input logic high	$V_{IH.CA.AC125}$	V_{REF} + 0.125	See 2)	V	1)
AC input logic low	$V_{IL.CA.AC125}$	See 2)	V_{REF} - 0.125	V	1)

Parameter	Symbol	DDR3L-1866,2133		Unit	Note
		Min.	Max.		
DC input logic high	$V_{IH.CA.DC90}$	V_{REF} + 0.09	V_{DD}	V	1)
DC input logic low	$V_{IL.CA.DC90}$	V_{SS}	V_{REF} - 0.09	V	1)
AC input logic high	$V_{IH.CA.AC160}$	-	-	V	1)
AC input logic low	$V_{IL.CA.AC160}$	-	-	V	1)
AC input logic high	$V_{IH.CA.AC135}$	V_{REF} + 0.135	See 2)	V	1)
AC input logic low	$V_{IL.CA.AC135}$	See 2)	V_{REF} - 0.135	V	1)
AC input logic high	$V_{IH.CA.AC125}$	V_{REF} + 0.125	See 2)	V	1)
AC input logic low	$V_{IL.CA.AC125}$	See 2)	V_{REF} - 0.125	V	1)

1) For input only pins except RESET: $V_{REF} = V_{REF.CA(DC)}$
2) See **Chapter 3.9 Overshoot and Undershoot Specification**.

Table 16 - DC and AC Input Levels for Single-Ended DQ and DM Signals

Parameter	Symbol	DDR3-1866,2133	Unit	Unit	Note
		Min.	Max.		
DC input logic high	$V_{IH.DQ.DC100}$	V_{REF} + 0.100	V_{DD}	V	1)
DC input logic low	$V_{IL.DQ.DC100}$	V_{SS}	V_{REF} - 0.100	V	1)
AC input logic high	$V_{IH.DQ.AC175}$	-	-	V	1)
AC input logic low	$V_{IL.DQ.AC175}$	-	-	V	1)
AC input logic high	$V_{IH.DQ.AC150}$	-	-	V	1)
AC input logic low	$V_{IL.DQ.AC150}$	-	-	V	1)
AC input logic high	$V_{IH.DQ.AC135}$	V_{REF} + 0.150	See 2)	V	1)
AC input logic low	$V_{IL.DQ.AC135}$	See 2)	V_{REF} - 0.150	V	1)

Parameter	Symbol	DDR3L-1866,2133	Unit	Unit	Note
		Min.	Max.		
DC input logic high	$V_{\text{IH.DQ.DC90}}$	V_{REF} + 0.09	V_{DD}	V	1)
DC input logic low	$V_{\text{IL.DQ.DC90}}$	V_{SS}	V_{REF} - 0.09	V	1)
AC input logic high	$V_{\text{IH.DQ.AC135}}$	-	-	V	1)
AC input logic low	$V_{\text{IL.DQ.AC135}}$	-	-	V	1)
AC input logic high	$V_{\text{IH.DQ.AC130}}$	V_{REF} + 0.130	See 2)	V	1)
AC input logic low	$V_{\text{IL.DQ.AC130}}$	See 2)	V_{REF} - 0.130	V	1)

1) For DQ and DM: $V_{\text{REF}} = V_{\text{REFDQ(DC)}}$
2) See **Chapter 3.9 Overshoot and Undershoot Specification**.

Differential Swing Requirement for Differential Signals

Table 17 shows the input levels for differential input signals.

Table 17 - Differential swing requirement for clock (CK - CK#) and strobe (DQS - DQS#)

Parameter	Symbol	DDR3-1866/2133		Unit	Note
		Min.	Max.		
Differential input high	$V_{\text{IH.DIFF}}$	+0.200	See 1)	V	2)
Differential input low	$V_{\text{IL.DIFF}}$	See1)	–0.200	V	2)
Differential input high AC	$V_{\text{IH.DIFF.AC}}$	2 x ($V_{\text{IH.AC}}$ - V_{REF}) 3)	See 1)	V	4)
Differential input low AC	$V_{\text{IL.DIFF.AC}}$	See 1)	2 x ($V_{\text{IL.AC}}$ - V_{REF}) 5)	V	4)

Parameter	Symbol	DDR3L-1866/2133		Unit	Note
		Min.	Max.		
Differential input high	$V_{\text{IH.DIFF}}$	+0.180	See 1)	V	2)
Differential input low	$V_{\text{IL.DIFF}}$	See1)	–0.180	V	2)
Differential input high AC	$V_{\text{IH.DIFF.AC}}$	2 x ($V_{\text{IH.AC}}$ - V_{REF}) 3)	See 1)	V	4)
Differential input low AC	$V_{\text{IL.DIFF.AC}}$	See 1)	2 x ($V_{\text{IL.AC}}$ - V_{REF}) 5)	V	4)

1) These values are not defined, however they single-ended signals CK, CK#, DQS, DQS# need to be within the respective limits ($V_{\text{IH.DC.MAX}}$, $V_{\text{IL.DC.MIN}}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Chapter 3.9.
2) Used to define a differential signal slew-rate.
3) Clock: us e VIH.CA.AC for VIH.AC. Strobe: use VIH.DQ.AC for VIH.AC.
4) For CK - CK# use VIH /VIL.AC of ADD/CMD and VREFCA; for DQS - DQS# use VIH /VIL.AC of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
5) Clock: use VIL.CA.AC for VIL.AC. Strobe: use VIL.DQ.AC for VIL.AC.

Table 18 - Allowed Time Before Ringback (tDVAC) for CK - CK# and DQS – DQS#

Slew Rate [V/ns]	DDR3-1866/2133			
	t_{DVAC} [ps] @ $\lvert V_{IH/IL.DIFF.AC} \rvert$ = 300mV		t_{DVAC} [ps] @ $\lvert V_{IH/IL.DIFF.AC} \rvert$ = (CK – CKS#) only	
	Min.	Max.	Min.	Max.
> 4.0	134	—	139	—
4.0	134	—	139	—
3.0	112	—	118	—
2.0	67	—	77	—
1.8	52	—	63	—
1.6	33	—	45	—
1.4	9	—	23	—
1.2	note	—	note	—
1.0	note	—	note	—
<1.0	note	—	note	—
Note: Rising input differential signal shall become equal to or greater than VIHdiff(ac) level and Falling input differential signal shall become equal to or less than VILdiff(ac) level.				

Slew Rate [V/ns]	DDR3L-1866/2133					
	t_{DVAC} [ps] @ $\lvert V_{IH/IL.DIFF.AC} \rvert$ = 270mV		t_{DVAC} [ps] @ $\lvert V_{IH/IL.DIFF.AC} \rvert$ = 250mV		t_{DVAC} [ps] @ $\lvert V_{IH/IL.DIFF.AC} \rvert$ = 260mV	
	Min.	Max.	Min.	Max.	Min.	Max.
> 4.0	163	—	168	—	176	—
4.0	163	—	168	—	176	—
3.0	140	—	147	—	154	—
2.0	95	—	105	—	111	—
1.8	80	—	91	—	97	—
1.6	62	—	74	—	78	—
1.4	37	—	52	—	56	—
1.2	5	—	22	—	24	—
1.0	note	—	note	—	note	—
<1.0	note	—	note	—	note	—
Note: Rising input differential signal shall become equal to or greater than VIHdiff(ac) level and Falling input differential signal shall become equal to or less than VILdiff(ac) level.						

Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, CK#, DQS#,) has also to comply with certain requirements for single-ended signals.

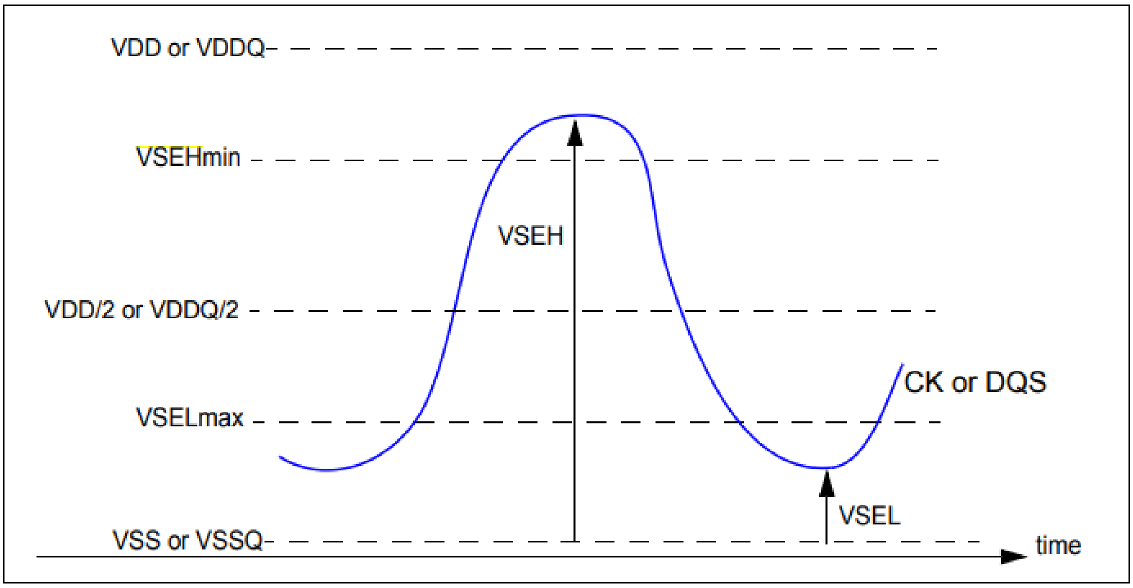
CK and CK# have to approximately reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately equal to the ac-levels ($V_{IH.AC}$ / $V_{IL.AC}$) for ADD/CMD signals) in every half-cycle. DQS, DQS# have to reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately the ac-levels ($V_{IH.AC}$ / $V_{IL.AC}$) for DQ signals) in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQs might be different per speed-bin etc.

E.g. if $V_{IH150.AC}$ / $V_{IL150.AC}$ is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and

CK#.

Figure 3 - Single ended requirement for differential signals



Note that while ADD/CMD and DQ signal requirements are with respect to V_{ref}, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time.

For single-ended components of differential signals the requirement to reach $V_{SEL.MAX}$, $V_{SEH.MIN}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 19 - Each Single-Ended Levels for CK, DQS, DQS#, CK#

Parameter	Symbol	DDR3(L)-1866, 2133		Unit	Note
		Min.	Max.		
Single-ended high-level for strobes	V_{SEH}	(VDDQ/2)+0.175	See [1]	V	2)3)
Single-ended high-level for CK, CK#	V_{SEH}	(VDD/2)+0.175	See [1]	V	
Single-ended low-level for strobes	V_{SEL}	See [1]	(VDDQ/2)-0.175	V	
Single-ended low-level for CK, CK#	V_{SEL}	See [1]	(VDD/2)-0.175	V	

1) These values are not defined, however they single-ended signals CK, CK#, DQS, DQS# need to be within the respective limits ($V_{IH.DC.MAX}$, $V_{IL.DC.MIN}$) for single-ended signals as well as the limitations for overshoot and undershoot.
2) For CK, CK# use $V_{IH.AC}$ /$V_{IL.AC}$ of ADD/CMD; for strobes (DQS, DQS#) use $V_{IH.AC}$/$V_{IL.AC}$ of DQs.
3) $V_{IH.AC}$/$V_{IL.AC}$ for DQs is based on V_{REFDQ}; $V_{IH.AC}$/$V_{IL.AC}$ for ADD/CMD is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK and DQS, DQS) must meet the requirements in the following table. The differential input cross point voltage VIX is measured from the actual cross point of true and complete signal to the midlevel between of VDD and VSS.

VIX Definition

Figure 4 - Vix definition

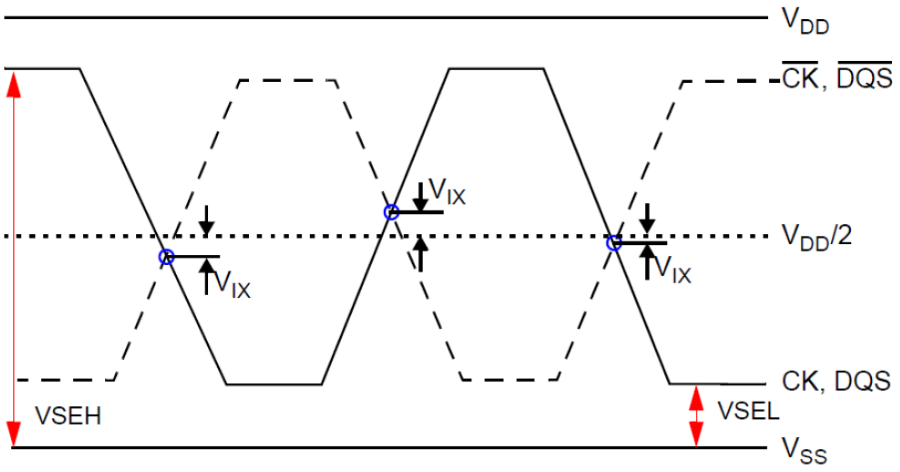


Table 20 - Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3-1866, 2133		DDR3L-1866, 2133		Unit	Note
		Min.	Max.	Min.	Max.		
V_{IX} (CK)	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK – CK#	–150	150	–150	150	mV	2)
		–175	175	-	-	mV	1)
V_{IX}(DQS)	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS –DQS#	–150	150	–150	150	mV	2)

1) Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic, have a single-ended swing V_{SEL}/V_{SEH} (see **Single-Ended Requirements for Differential Signals**) of at least $V_{DD}/2$ +/-250 mV and if the differential slew rate of CK - CK# is larger than 3 V/ns.

2) the relation between Vix min/max and VSEL/VSEH should satisfy following:
VDD/2+Vix(min)-VSEL ≥ 25mv
VSEH-(VDD/2+Vix(max)) ≥ 25mv

DC and AC Output Measurements Levels

Table 21 - DC and AC Output Levels for Single-Ended Signals

Parameter	Symbol	DDR3(L)-1866,2133	Unit	Note
DC output high measurement level (for IV curve linearity)	$V_{OH.DC}$	0.8 x V_{DDQ}	V	
DC output mid measurement level (for IV curve linearity)	$V_{OM.DC}$	0.5 x V_{DDQ}	V	
DC output low measurement level (for IV curve linearity)	$V_{OL.DC}$	0.2 x V_{DDQ}	V	
AC output high measurement level (for output slew rate)	$V_{OH.AC}$	V_{TT} + 0.1 x V_{DDQ}	V	1)
AC output low measurement level (for output slew rate)	$V_{OL.AC}$	V_{TT} - 0.1 x V_{DDQ}	V	1)

1) Background: the swing of ± 0.1 x V_{DDQ} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ} / 2$.

Table 22 - AC Output Levels for Differential Signals

Parameter	Symbol	DDR3(L)-1866,2133	Unit	Note
AC differential output high measurement level (for output slew rate)	$V_{OH.DIFF.AC}$	+0.2 x V_{DDQ}	V	1)
AC differential output low measurement level (for output slew rate)	$V_{OL.DIFF.AC}$	–0.2 x V_{DDQ}	V	1)

1) Background: the swing of ± 0.2 x V_{DDQ} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ} / 2$ at each of the differential outputs.

3.5 Output Slew Rates

Table 23 - Output Slew Rates

Parameter	Symbol	DDR3-1866, 2133		DDR3L-1866, 2133		Unit	Note
		Min.	Max.	Min.	Max.		
Single-ended Output Slew Rate	SRQse	2.5	5	1.75	5	V / ns	1)2)
Differential Output Slew Rate	SRQdiff	5	12	3.5	12	V / ns	

1) For $R_{ON} = R_{ZQ}/7$ settings only.
2) Background for Symbol Nomenclature: SR: Slew Rate; Q: Query Output; se: single-ended; diff: differential.

3.6 ODT DC Impedance and Mid-Level Characteristics

Table 24 provides the ODT DC impedance and mid-level characteristics.

Table 24 - ODT DC Impedance and Mid-Level Characteristics

DDR3							
Symbol	Description	V_{OUT} Condition	Min.	Nom.	Max.	Unit	Note
R_{TT120}	R_{TT} effective = 120 Ω	$V_{IL.AC}$ and $V_{IH.AC}$	0.9	1.0	1.6	$R_{ZQ}/2$	1)2)3)4)
R_{TT60}	R_{TT} effective = 60 Ω		0.9	1.0	1.6	$R_{ZQ}/4$	1)2)3)4)
R_{TT40}	R_{TT} effective = 40 Ω		0.9	1.0	1.6	$R_{ZQ}/6$	1)2)3)4)
R_{TT30}	R_{TT} effective = 30 Ω		0.9	1.0	1.6	$R_{ZQ}/8$	1)2)3)4)
R_{TT20}	R_{TT} effective = 20 Ω		0.9	1.0	1.6	$R_{ZQ}/12$	1)2)3)4)
ΔV_M	Deviation of V_M with respect to V_{DDQ} / 2	floating	–5	—	+5	%	1)2)3)4)5)

DDR3L							
Symbol	Description	V_{OUT} Condition	Min.	Nom.	Max.	Unit	Note
R_{TT120}	R_{TT} effective = 120 Ω	$V_{IL.AC}$ and $V_{IH.AC}$	0.9	1.0	1.65	$R_{ZQ}/2$	1)2)3)4)
R_{TT60}	R_{TT} effective = 60 Ω		0.9	1.0	1.65	$R_{ZQ}/4$	1)2)3)4)
R_{TT40}	R_{TT} effective = 40 Ω		0.9	1.0	1.65	$R_{ZQ}/6$	1)2)3)4)
R_{TT30}	R_{TT} effective = 30 Ω		0.9	1.0	1.65	$R_{ZQ}/8$	1)2)3)4)
R_{TT20}	R_{TT} effective = 20 Ω		0.9	1.0	1.65	$R_{ZQ}/12$	1)2)3)4)
ΔV_M	Deviation of V_M with respect to V_{DDQ} / 2	floating	–5	—	+5	%	1)2)3)4)5)

1) With R_{ZQ} = 240 Ω.
2) Measurement definition for R_{TT} : Apply $V_{IH.AC}$ and $V_{IL.AC}$ to test ball separately, then measure current I ($V_{IH.AC}$) and I ($V_{IL.AC}$) respectively.
$R_{TT} = [V_{IH.AC} - V_{IL.AC}] / [I (V_{IH.AC}) - I (V_{IL.AC})]$
3) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the **ODT DC Impedance Sensitivity on Temperature and Voltage Drifts**.
4) The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
5) Measurement Definition for ΔV_M: Measure voltage (V_M) at test ball (midpoint) with no load: $\Delta V_M = (2 \times V_M / V_{DDQ} - 1) \times 100\%$.

3.7 ODT DC Impedance Sensitivity on Temperature and Voltage Drifts

If temperature and/or voltage change after calibration, the tolerance limits widen for R_{TT} according to the following tables. The following definitions are used:
$\Delta T = T - T$ (at calibration); $\Delta V = V_{DDQ} - V_{DDQ}$ (at calibration); $V_{DD} = V_{DDQ}$

Table 25 - ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift

Symbol	Value		Unit	Note
	Min.	Max.		
R_{TT}	0.9 - dR_{TT}dT x |ΔT| - dR_{TT}dV x |ΔV|	1.6 + dR_{TT}dT x |ΔT| + dR_{TT}dV x |ΔV|	R_{ZQ} / $TISF_{RTT}$	1)

1) $TISF_{RTT}$: Termination Impedance Scaling Factor for R_{TT}:
$TISF_{RTT}$ = 12 for R_{TT020}
$TISF_{RTT}$ = 8 for R_{TT030}
$TISF_{RTT}$ = 6 for R_{TT040}
$TISF_{RTT}$ = 4 for R_{TT060}
$TISF_{RTT}$ = 2 for R_{TT120}

Table 26 - OTD DC Impedance Sensitivity Parameters

Symbol	Value		Unit	Note
	Min.	Max.		
dR_{TT}dT	0	1.5	%/°C	1)
dR_{TT}dV	0	0.15	%/mV	

1) These parameters may not be subject to production test. They are verified by design and characterization.

3.8 Interface Capacitance

Definition and values for interface capacitances are provided in the following table.

Table 27 - Interface Capacitance Values

parameter	signal	Symbol	DDR3(L)–1866		DDR3(L)–2133		Unit	Note
			Min.	Max.	Min.	Max.		
Input/Output Capacitance	DQ, DM, DQS, DQS#	C_{IO}(DDR3)	1.4	2.2	1.4	2.1	pF	1)2)3)
		C_{IO}(DDR3L)	1.4	2.1	1.4	2.1	pF	1)2)3)
Input Capacitance	CK, CK#	C_{CK}	0.8	1.3	0.8	1.3	pF	2)3)
Input Capacitance Delta	CK, CK#	C_{DCK}	0	0.15	0	0.15	pF	2)3)4)
Input/Output Capacitance delta DQS and DQS#	DQS, DQS#	C_{DDQS}	0	0.2	0	0.15	pF	2)3)5)
Input Capacitance	All other input-only pins	C_{I}	0.75	1.2	0.75	1.2	pF	2)3)6)
Input Capacitance delta	All CTRL input-only pins	$C_{\mathrm{DI\_CTRL}}$	–0.4	0.2	–0.4	0.2	pF	2)3)7)8)
Input Capacitance delta	All ADD and CMD input-only pins	$C_{\mathrm{DI\_ADD\_CMD}}$	–0.4	0.4	–0.4	0.4	pF	2)3)9)10)
Input/Output Capacitance delta	DQ,DM,DQS, DQS#	C_{DIO}	–0.5	0.3	–0.5	0.3	pF	2)3)11)
ZQ Capacitance	ZQ	C_{ZQ}	–	3	–	3	pF	12)

1) Although the DM signal has different function, the loading matches DQ and DQS
2) This parameter is not subject to production test. It is verified by design and characterization. Capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other balls floating (except the ball under test, CKE, RESET# and ODT as necessary). $V_{\mathrm{DD}} = V_{\mathrm{DDQ}} = 1.5$ V, $V_{\mathrm{BIAS}} = V_{\mathrm{DD}}/2$ and on-die termination off
3) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4) Absolute value of C_{CK} - $C_{\mathrm{CK\#}}$
5) Absolute value of $C_{\mathrm{IO.DQS}}$ - $C_{\mathrm{IO.DQS\#}}$
6) C_{I} applies to ODT, CS#, CKE, A[15:0], BA[2:0], RAS#, CAS#, WE#
7) $C_{\mathrm{DI\_CTRL}}$ applies to ODT, CS# and CKE
8) $C_{\mathrm{DI\_CTRL}} = C_{\mathrm{I.CTRL}} - 0.5 \times (C_{\mathrm{I.CK}} + C_{\mathrm{I.CK\#}})$
9) $C_{\mathrm{DI\_ADD\_CMD}}$ applies to A[15:0], BA[2:0], RAS#, CAS# and WE#
10) $C_{\mathrm{DI\_ADD\_CMD}} = C_{\mathrm{I.ADD,CMD}} - 0.5 \times (C_{\mathrm{I.CK}} + C_{\mathrm{I.CK\#}})$
11) $C_{\mathrm{DIO}} = C_{\mathrm{IO.DQ,DM}} - 0.5 \times (C_{\mathrm{IO.DQS}} + C_{\mathrm{IO.DQS\#}})$
12) Maximum external load capacitance on ZQ signal: 5 pF

3.9 Overshoot and Undershoot Specification

Table 28 - AC Overshoot / Undershoot Specification for Address and Control Signals

Parameter	DDR3(L)–1866	DDR3(L)–2133	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	V	1)2)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	V	1)3)
Maximum overshoot area above V_{DD}	0.28	0.25	V × ns	1)
Maximum undershoot area below V_{SS}	0.28	0.25	V × ns	1)

1) Applies for the following signals: A[12:0], BA[2:0], CS#, RAS#, CAS#, WE#, CKE and ODT
2) The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
3) The sum of applied voltage (VDD) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings

Figure 5 - AC Overshoot / Undershoot Definitions for Address and Control Signals

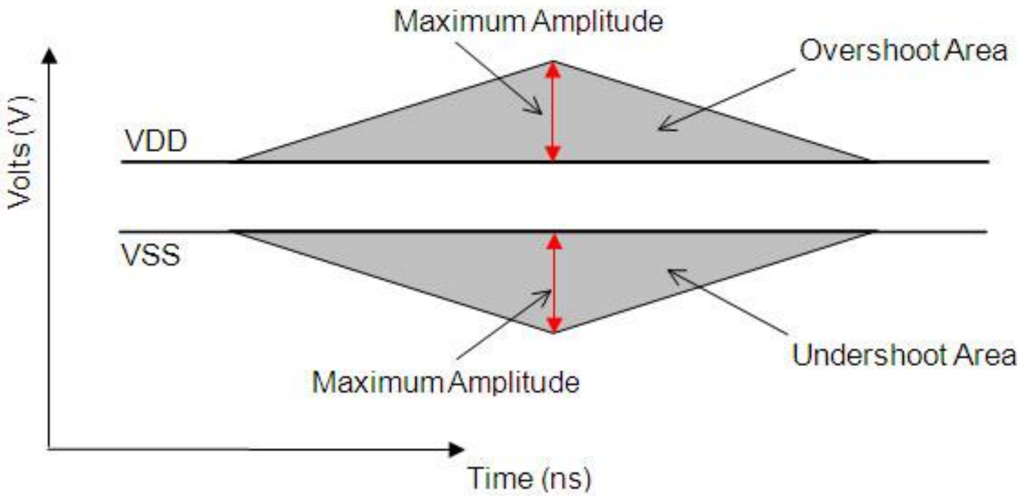
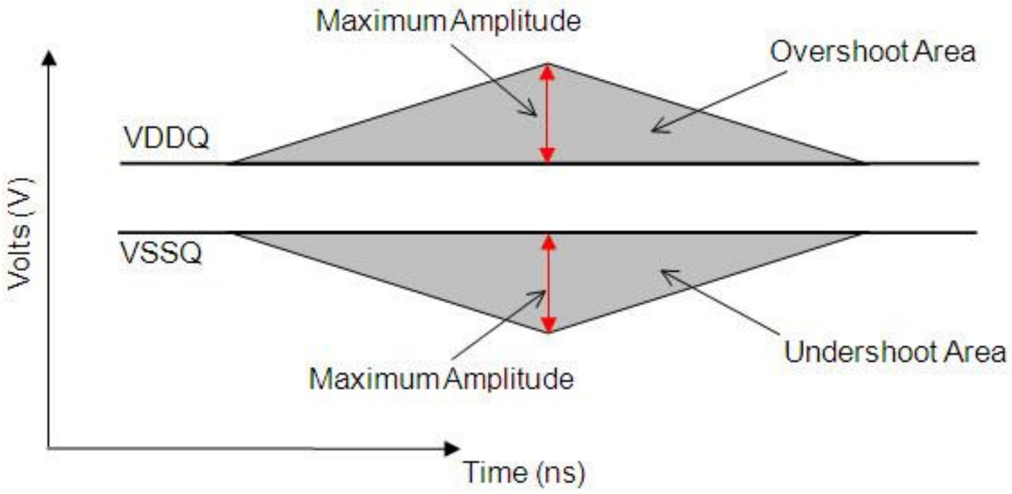


Table 29 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals

Parameter	DDR3(L)–1866	DDR3(L)–2133	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	V	1)2)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	V	1)3)
Maximum overshoot area above V_{DDQ}	0.11	0.10	V × ns	1)
Maximum undershoot area below V_{SSQ}	0.11	0.10	V × ns	1)

1) Applies for CK, CK#, DQ, DQS, DQS# & DM
2) The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
3) The sum of applied voltage (VDD) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.

Figure 6 - AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals



4 Electrical Specifications

Table 30 - IDD Specification parameters and test conditions (V_{DD} = 1.35V)

Parameter & Test Condition	Symbol	1866	2133	Unit
		Max		
Operating One Bank Active-Precharge Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...;**Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD0}	75	77	mA
Operating One Bank Active-Read-Precharge Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 5]; **AL:**0; **CS#**: High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD1}	86	90	mA
Precharge Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD2N}	52	55	mA
Precharge Power-Down Current Slow Exit **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Slow Exit.[*3]	I_{DD2P0}	16	16	mA
Precharge Power-Down Current Fast Exit **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Fast Exit.[*3]	I_{DD2P1}	19	19	mA
Precharge Quiet Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD2Q}	52	55	mA
Active Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD3N}	62	64	mA
Active Power-Down Current **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0	I_{DD3P}	24	25	mA
Operating Burst Read Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 5]; **AL:** 0; **CS#**: High between RD; **Command, Address, Bank Address Inputs:** partially toggling; **DM**:stable at 0; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; **output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD4R}	140	155	mA

Parameter & Test Condition		Symbol	1866	2133	Unit
			Max		
Operating Burst Write Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between WR; **Command, Address, Bank Address Inputs:** partially toggling; **DM:** stable at 0; **Bank Activity:** all banks open. **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at HIGH.		I_{DD4W}	155	168	mA
Burst Refresh Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between tREF; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** REF command every tRFC; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.		I_{DD5B}	97	100	mA
Self Refresh Current: **Self-Refresh Temperature Range (SRT):** Normal[4]; **CKE:** Low; **External clock:** Off; CK and CK#: LOW; **BL:** 8[*1]; **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** MID-LEVEL	***T*CASE:** 0 - 85°C	I_{DD6}	13	14	mA
	***T*CASE:** 0 - 95°C	I_{DD6ET}	15	16	mA
Operating Bank Interleave Read Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 5]; **AL:** CL-1; **CS#**: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling; **DM**:stable at 0; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.		I_{DD7}	150	160	mA
RESET Low Current **RESET:** LOW; **External clock:** Off; **CK and CK#:** LOW; **CKE:** FLOATING; **CS#, Command, Address, Bank Address, Data IO:** FLOATING; **ODT Signal:** FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.		I_{DD8}	10	10	mA

Table 31 - IDD Specification parameters and test conditions (V_{DD} = 1.5V)

Parameter & Test Condition	Symbol	1866	2133	Unit
		Max		
Operating One Bank Active-Precharge Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...;**Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD0}	75	77	mA
Operating One Bank Active-Read-Precharge Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 5]; **AL:**0; **CS#**: High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD1}	90	96	mA
Precharge Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD2N}	55	59	mA
Precharge Power-Down Current Slow Exit **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Slow Exit.[*3]	I_{DD2P0}	18	19	mA

Parameter & Test Condition		Symbol	1866	2133	Unit
			Max		
Precharge Power-Down Current Fast Exit **CKE:** Low; **External clock:** On; **BL:** 8^{*1}; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Fast Exit.^{*3}		I_{DD2P1}	19	19	mA
Precharge Quiet Standby Current **CKE**: High; **External clock:** On; **BL:** 8^{*1}; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** stable at 0.		I_{DD2Q}	55	59	mA
Active Standby Current **CKE**: High; **External clock:** On; **BL:** 8^{*1}; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** stable at 0.		I_{DD3N}	62	64	mA
Active Power-Down Current **CKE:** Low; **External clock:** On; **BL:** 8^{*1}; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** stable at 0		I_{DD3P}	24	25	mA
Operating Burst Read Current **CKE:** High; **External clock:** On; **BL:** $8^{*1,\ 5}$; **AL:** 0; **CS#**: High between RD; **Command, Address, Bank Address Inputs:** partially toggling; **DM**:stable at 0; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; **output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** stable at 0.		I_{DD4R}	143	155	mA
Operating Burst Write Current **CKE:** High; **External clock:** On; **BL:** 8^{*1}; **AL:** 0; **CS#**: High between WR; **Command, Address, Bank Address Inputs:** partially toggling; **DM:** stable at 0; **Bank Activity:** all banks open. **Output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** stable at HIGH.		I_{DD4W}	156	168	mA
Burst Refresh Current **CKE:** High; **External clock:** On; **BL:** 8^{*1}; **AL:** 0; **CS#**: High between tREF; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** REF command every tRFC; **Output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** stable at 0.		I_{DD5B}	97	100	mA
Self Refresh Current: **Self-Refresh Temperature Range (SRT):** Normal^{4}; **CKE:** Low; **External clock:** Off; CK and CK#: LOW; **BL:** 8^{*1}; **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** MID-LEVEL	***T*CASE:** 0 - 85°C	I_{DD6}	13	14	mA
	***T*CASE:** 0 - 95°C	I_{DD6ET}	15	16	mA
Operating Bank Interleave Read Current **CKE:** High; **External clock:** On; **BL:** $8^{*1,\ 5}$; **AL:** CL-1; **CS#**: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling; **DM**:stable at 0; **Output Buffer and RTT:** Enabled in Mode Registers^{*2}; **ODT Signal:** stable at 0.		I_{DD7}	150	160	mA
RESET Low Current **RESET:** LOW; **External clock:** Off; **CK and CK#:** LOW; **CKE:** FLOATING; **CS#, Command, Address, Bank Address, Data IO:** FLOATING; **ODT Signal:** FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.		I_{DD8}	10	12	mA

Note 1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B.

Note 2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B.

Note 3. Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit.

Note 4. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range.

Note 5. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B.

Note 6. Supporting 0 - 85 °C with full JEDEC AC & DC specifications. This is the minimum requirements for all operating temperature options. However, for applications operating in Extended Temperature 85°C ~ 95°C, some optional spec are required.

5 Electrical Characteristics and Recommended A.C. Operating Conditions

Table 32 - Electrical Characteristics and Recommended A.C. Operating Conditions

Symbol	Parameter		DDR3(L)-1866		DDR3(L)-2133		Unit	Note
			Min.	Max.	Min.	Max.		
t_{AA}	Internal read command to first data		13.91	20	13.09	20	ns	
t_{RCD}	ACT to internal read or write delay time		13.91		13.09	-	ns	
t_{RP}	PRE command period		13.91		13.09	-	ns	
t_{RC}	ACT to ACT or REF command period		47.91		46.09	-	ns	
t_{RAS}	ACTIVE to PRECHARGE command period		34	9 x t_{REFI}	33	9 x t_{REFI}	ns	
$t_{CK(avg)}$	Average clock period	CL=5, CWL=5	-	-	-	-	ns	33
		CL=6, CWL=5	2.5	3.3	2.5	3.3	ns	33
		CL=7, CWL=6	1.875	<2.5	1.875	<2.5	ns	33
		CL=8, CWL=6	1.875	<2.5	1.875	<2.5	ns	33
		CL=9, CWL=7	1.5	<1.875	1.5	<1.875	ns	33
		CL=10, CWL=7	1.5	<1.875	1.5	<1.875	ns	33
		CL=11, CWL=8	1.25	<1.5	1.25	<1.5	ns	33
		CL=13, CWL=9	1.07	<1.25	1.07	<1.25	ns	33
		CL=14 CWL=10	-	-	0.938	<1.07	ns	33
$t_{CK\ (DLL\_OFF)}$	Minimum Clock Cycle Time (DLL off mode)		8	-	8	-	ns	6
$t_{CH(avg)}$	Average clock HIGH pulse width		0.47	0.53	0.47	0.53	t_{CK}	
$t_{CL(avg)}$	Average Clock LOW pulse width		0.47	0.53	0.47	0.53	t_{CK}	
t_{DQSQ}	DQS, DQS# to DQ skew, per group, per access		-	85	-	75	ps	13
t_{QH}	DQ output hold time from DQS, DQS#		0.38	-	0.38	-	t_{CK}	13
$t_{LZ(DQ)}$	DQ low-impedance time from CK, CK#		-390	195	-360	180	ps	13,14
$t_{HZ(DQ)}$	DQ high impedance time from CK, CK#		-	195	-	180	ps	13,14
$t_{DS(base)}$	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	AC150(DDR3)	-	-	-	-	ps	17
		AC135(DDR3)	68	-	53	-	ps	17
		AC135(DDR3L) SR = 1V/ns	-	-	-	-	ps	17
		AC130(DDR3L) SR = 2V/ns	70	-	55		ps	17
$t_{DH(base)}$	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	DC100(DDR3)	-	-	-	-	ps	17
		DC90(DDR3L) SR = 1V/ns	-	-	-	-	ps	17
		DC90(DDR3L) SR = 2V/ns	75	-	60		ps	17
t_{DIPW}	DQ and DM Input pulse width for each input		320	-	280	-	ps	
t_{RPRE}	DQS,DQS# differential READ Preamble		0.9	-	0.9	-	t_{CK}	13,19
t_{RPST}	DQS, DQS# differential READ Postamble		0.3	-	0.3	-	t_{CK}	11,13
t_{QSH}	DQS, DQS# differential output high time		0.4	-	0.4	-	t_{CK}	13
t_{QSL}	DQS, DQS# differential output low time		0.4	-	0.4	-	t_{CK}	13
t_{WPRE}	DQS, DQS# differential WRITE Preamble		0.9	-	0.9	-	t_{CK}	1
t_{WPST}	DQS, DQS# differential WRITE Postamble		0.3	-	0.3	-	t_{CK}	1
t_{DQSCK}	DQS, DQS# rising edge output access time from rising CK, CK#		-195	195	-180	180	ps	13

Symbol	Parameter		DDR3(L)-1866		DDR3(L)-2133		Unit	Note
			Min.	Max.	Min.	Max.		
$t_{LZ(DQS)}$	DQS and DQS# low-impedance time (Referenced from RL - 1)		-390	195	-360	180	ps	13, 14
$t_{HZ(DQS)}$	DQS and DQS# high-impedance time (Referenced from RL + BL/2)		-	195	-	180	ps	13, 14
t_{DQSL}	DQS, DQS# differential input low pulse width		0.45	0.55	0.45	0.55	t_{CK}	29, 31
t_{DQSH}	DQS, DQS# differential input high pulse width		0.45	0.55	0.45	0.55	t_{CK}	30, 31
t_{DQSS}	DQS, DQS# rising edge to CK, CK# rising edge		-0.27	0.27	-0.27	0.27	t_{CK}	
t_{DSS}	DQS, DQS# falling edge setup time to CK, CK# rising edge		0.18	-	0.18	-	t_{CK}	32
t_{DSH}	DQS, DQS# falling edge hold time from CK, CK# rising edge		0.18	-	0.18	-	t_{CK}	32
t_{DLLK}	DLL locking time		512	-	512	-	t_{CK}	
t_{RTP}	Internal READ Command to PRECHARGE Command delay		max (4tCK, 7.5ns)	-	max (4tCK, 7.5ns)	-	tCK	
t_{WTR}	Delay from start of internal write transaction to internal read command		max (4tCK, 7.5ns)	-	max (4tCK, 7.5ns)	-	tCK	18
t_{WR}	WRITE recovery time		15	-	15	-	ns	18
t_{MRD}	Mode Register Set command cycle time		4	-	4	-	tCK	
t_{MOD}	Mode Register Set command update delay		max (12tCK, 15ns)	-	max (12tCK, 15ns)	-	tCK	
t_{CCD}	CAS# to CAS# command delay		4	-	4	-	tCK	
$t_{DAL(min)}$	Auto precharge write recovery + prechargetime		WR + round up(t_{RP} / Tck(avg))				t_{CK}	
t_{MPRR}	Multi-Purpose Register Recovery Time		1	-	1	-	t_{CK}	22
t_{RRD}	ACTIVE to ACTIVE command period		max (4t_{CK},6ns)	-	Max (4t_{CK},6ns)	-	t_{CK}	
t_{FAW}	Four activate window		35	-	35	-	ns	
$t_{IS(base)}$	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	AC175(DDR3)	-	-	-	-	ps	16
		AC150(DDR3)	-	-	-	-	ps	16,27
		AC125(DDR3)	150	-	135	-	ps	16,27
		AC160(DDR3L) SR = 1V/ns	-	-	-	-	ps	16
		AC135(DDR3L) SR = 1V/ns	65	-	60	-	ps	16
		AC125(DDR3L) SR = 1V/ns	150	-	135	-	ps	16
$t_{IH(base)}$	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	DC90(DDR3)	100	-	95	-	ps	16
		DC90(DDR3L) SR = 1V/ns	110	-	105	-	ps	16
t_{IPW}	Control and Address Input pulse width for each input		535		470	-	ps	28
t_{ZQinit}	Power-up and RESET calibration time		512	-	512	-	t_{CK}	
t_{ZQoper}	Normal operation Full calibration time		256	-	256	-	t_{CK}	
t_{ZQCS}	Normal operation Short calibration time		64	-	64	-	t_{CK}	23
t_{XPR}	Exit Reset from CKE HIGH to a valid command		max (5t_{CK}, $t_{RFC(min)}$ + 10ns)	-	max (5t_{CK}, $t_{RFC(min)}$ + 10ns)	-	t_{CK}	

Symbol	Parameter	DDR3(L)-1866		DDR3(L)-2133		Unit	Note
		Min.	Max.	Min.	Max.		
t_{XS}	Exit Self Refresh to commands not requiring a locked DLL	max (5t_{CK}, $t_{RFC(min)}$ + 10ns)	-	max (5t_{CK}, $t_{RFC(min)}$ + 10ns)	-	t_{CK}	
t_{XSDLL}	Exit Self Refresh to commands requiring a locked DLL	$t_{DLLK(min)}$	-	$t_{DLLK(min)}$	-	t_{CK}	
t_{CKESR}	Minimum CKE low width for Self Refresh entry to exit timing	$t_{CKE(min)}$ + 1t_{CK}	-	$t_{CKE(min)}$ + 1t_{CK}	-	t_{CK}	
t_{CKSRE}	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	max (5t_{CK}, 10 ns)	-	max (5t_{CK}, 10 ns)	-	t_{CK}	
t_{CKSRX}	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	max (5t_{CK}, 10 ns)	-	max (5t_{CK}, 10 ns)	-	t_{CK}	
t_{XP}	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max (3t_{CK}, 6 ns)	-	max (3t_{CK}, 6 ns)	-	t_{CK}	
t_{XPDLL}	Exit Precharge Power Down with DLL frozen to commands requiring a lockedDLL	Max (10t_{CK}, 24ns)	-	Max (10t_{CK}, 24ns)	-	t_{CK}	2
t_{CKE}	CKE minimum pulse width	Max (3t_{CK},5ns)	-	Max (3t_{CK}, 5ns)	-	t_{CK}	
t_{CPDED}	Command pass disable delay	2	-	2	-	t_{CK}	
t_{PD}	Power Down Entry to Exit Timing	$t_{CKE\ (min)}$	9 x t_{REFI}	$t_{CKE\ (min)}$	9 x t_{REFI}		15
$t_{ACTPDEN}$	Timing of ACT command to Power Down entry	1	-	2	-	t_{CK}	20
t_{PRPDEN}	Timing of PRE or PREA command to Power Down entry	1	-	2	-	t_{CK}	20
t_{RDPDEN}	Timing of RD/RDA command to Power Down entry	RL+4+1	-	RL+4+1	-	t_{CK}	
t_{WRPDEN}	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL+4+ (tWR/tCK)	-	WL+4+ (tWR/tCK)	-	tCK	9
$t_{WRAPDEN}$	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS,BC4OTF)	WL+4+ WR+1	-	WL+4+ WR+1	-	tCK	10
t_{WRPDEN}	Timing of WR command to Power Down entry (BC4MRS)	WL+2+ (tWR/tCK)	-	WL+2+ (tWR/tCK)	-	tCK	9
$t_{WRAPDEN}$	Timing of WRA command to Power Down entry (BC4MRS)	WL+2+ WR+1	-	WL+2+ WR+1	-	tCK	10
$t_{REFPDEN}$	Timing of REF command to Power Down entry	1	-	1	-	tCK	20, 21
$t_{MRSPDEN}$	Timing of MRS command to Power Down entry	tMOD(min)	-	tMOD(min)	-		
ODTLon	ODT turn on Latency	WL - 2 = CWL + AL - 2				t_{CK}	
ODTLoff	ODT turn off Latency	WL - 2 = CWL + AL - 2					
ODTH4	ODT high time without write command or with write command and BC4	4	-	4	-	t_{CK}	
ODTH8	ODT high time with Write command and BL8	6	-	6	-	t_{CK}	
t_{AONPD}	Asynchronous RTT turn-on delay (Power- Down with DLL frozen)	2	8.5	2	8.5	ns	
t_{AOFPD}	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	2	8.5	ns	
t_{AON}	RTT turn-on	-195	195	-180	180	ps	7
t_{AOF}	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	t_{CK}	8
t_{ADC}	RTT dynamic change skew	0.3	0.7	0.3	0.7	t_{CK}	

Symbol	Parameter		DDR3(L)-1866		DDR3(L)-2133		Unit	Note
			Min.	Max.	Min.	Max.		
t_{WLMRD}	First DQS/DQS# rising edge after write leveling mode is programmed		40	-	40	-	t_{CK}	3
$t_{WLDQSEN}$	DQS/DQS# delay after write leveling mode is programmed		25	-	25	-	t_{CK}	3
t_{WLS}	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing		140	-	125	-	ps	
t_{WLH}	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing		140	-	125	-	ps	
t_{WLO}	Write leveling output delay		0	7.5	0	7.5	ns	
t_{WLOE}	Write leveling output error		0	2	0	2	ns	
t_{RFC}	REF command to ACT or REF command time		110	-	110	-	ns	
t_{REFI}	Average periodic refresh interval	0°C to 85°C	-	7.8	-	7.8	μs	
		85°C to 95°C	-	3.9	-	3.9	μs	

Note 1. Actual value dependant upon measurement level.

Note 2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

Note 3. The max values are system dependent.

Note 4. WR as programmed in mode register.

Note 5. Value must be rounded-up to next higher integer value.

Note 6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

Note 7. For definition of RTT turn-on time tAON See “Timing Parameters”.

Note 8. For definition of RTT turn-off time tAOF See “Timing Parameters”.

Note 9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.

Note 10. WR in clock cycles as programmed in MR0.

Note 11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See “Clock to Data Strobe Relationship”.

Note 12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.

Note 13. Value is only valid for RON34.

Note 14. Single ended signal parameter.

Note 15. tREFI depends on TOPER.

Note 16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See “Address / Command Setup, Hold and Derating”.

Note 17. tDS (base) and tDH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See “Data Setup, Hold and Slew Rate Derating”

Note 18. Start of internal write transaction is defined as follows:

- For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
- For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
- For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

Note 19. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See “Clock to Data Strobe Relationship”.

Note 20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

Note 21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See “Power-Down clarifications-Case 2”.

Note 22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

Note 23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’ and ‘ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

Where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

Note 24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

Note 25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

Note 26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Note 27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100ps of derating to accommodate for the lower altemate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV – 150mV) / 1V/ns].

Note 28. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).

Note 29. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.

Note 30. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.

Note 31. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

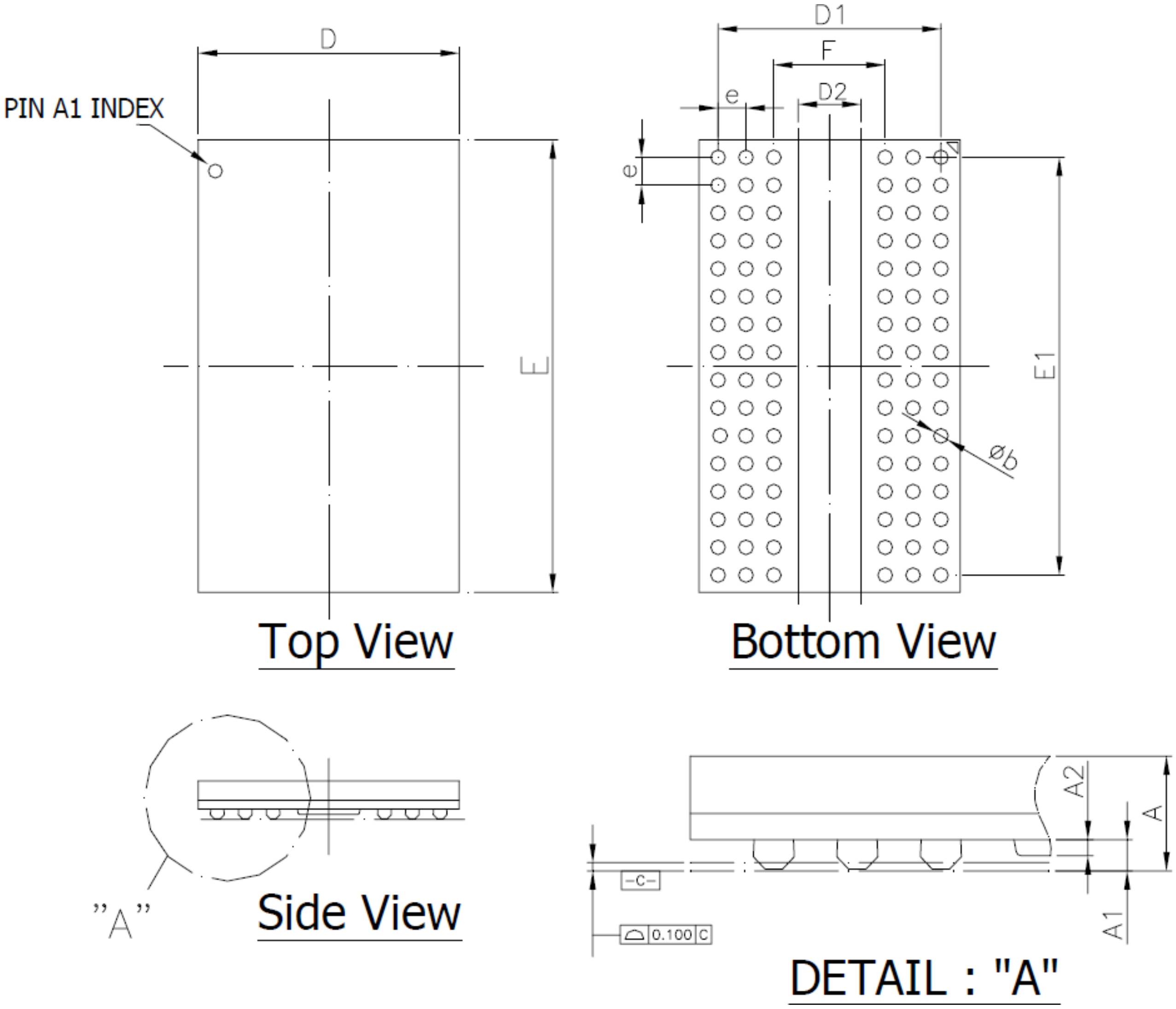
Note 32. tDQSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

Note 33. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled

6 Package Outlines

错误!未找到引用源。**7** reflects the current status of the outline dimensions of the DDR3(L) packages for 1Gbit component x16 configuration.

Figure 7 - 96-Ball FBGA Package 7.5x13x1.0 mm (max) Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.039	--	--	1.00
A1	0.012	**0.014**	0.016	0.30	0.35	0.40
A2	--	--	0.008	--	--	0.20
D	0.291	0.295	0.299	7.40	7.50	7.60
E	0.508	0.512	0.516	12.90	13.00	13.10
D1	--	0.252	--	--	6.40	--
E1	--	0.472	--	--	12.00	--
F	--	0.126	--	--	3.20	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
D2	--	--	0.081	--	--	2.05

7 Product Type Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter

Table 33 - DDR3(L) Memory Components

Field	Description	Values	Coding
1	UniIC Component Prefix	SCB	UniIC
2	Voltage	13	VDD, VDDQ=1.35V (1.283V ~ 1.45V)
3	DRAM Technology	H	DDR3
4	Density	1G	1 Gbit
5	Number of I/Os	16	X16
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
		D	Fourth
		E	Fifth
8	Package,	F	FBGA
9	Power	–	Standard power product
		L	Low power product
10	Speed Grade	11M	CL–Trcd–Trp =13-13-13
		09N	CL–Trcd–Trp =14-14-14
11	Temperature Range	Blank	Commercial Temperature Range:0~95℃
		I	Industiral Temperature:-40~95℃

List of Figures

Figure 1 - Ball out for 64 Mb ×16 Components (FBGA-96) 8
Figure 2 - Reference Load for AC Timings and Output Slew Rates 23
Figure 3 - Single ended requirement for differential signals 27
Figure 4 - Vix definition 28
Figure 5 - AC Overshoot / Undershoot Definitions for Address and Control Signals 32
Figure 6 - AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals 33
Figure 7 - 96-Ball FBGA Package 7.5x13x1.0 mm (max) Outline Drawing Information 43

List of Tables

Table 1 - Ordering Information for 1Gbit DDR3(L) Component 5
Table 2 - Input / Output Signal Functional Description 6
Table 3 - 1Gbit DDR3 SDRAM Addressing 9
Table 4 - Command Truth Table 10
Table 5 - Clock Enable (CKE) Truth Table for Synchronous Transitions 11
Table 6 - Data Mask (DM) Truth Table 12
Table 7 - MR0 Mode register Definition (BA[2:0]=000_B) 14
Table 8 - MR1 Mode Register Definition (BA[2:0]=001_B) 16
Table 9 - MR2 Mode Register Definition (BA[2:0]=010_B) 18
Table 10 - MR3 Mode Register Definition (BA[2:0]=011_B) 19
Table 11 - Bit Order during Burst 20
Table 12 - The relationship between tREFI and component Operating Temperature 21
Table 13 - Absolute Maximum Ratings 22
Table 14 - DC Operating Conditions 22
Table 15 - DC and AC Input Levels for Single-Ended Command, Address and Control Signals 24
Table 16 - DC and AC Input Levels for Single-Ended DQ and DM Signals 24
Table 17 - Differential swing requirement for clock (CK - CK#) and strobe (DQS - DQS#) 25
Table 18 - Allowed Time Before Ringback (tDVAC) for CK - CK# and DQS – DQS# 26
Table 20 - Each Single-Ended Levels for CK, DQS, DQS#, CK# 27
Table 21 - Cross Point Voltage for Differential Input Signals (CK, DQS) 28
Table 22 - DC and AC Output Levels for Single-Ended Signals 28
Table 23 - AC Output Levels for Differential Signals 28
Table 24 - Output Slew Rates 29
Table 25 - ODT DC Impedance and Mid-Level Characteristics 29
Table 26 - ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift 30
Table 27 - OTD DC Impedance Sensitivity Parameters 30
Table 28 - Interface Capacitance Values 31
Table 29 - AC Overshoot / Undershoot Specification for Address and Control Signals 32
Table 30 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals 32
Table 31 - IDD Specification parameters and test conditions (VDD = 1.35V) 34
Table 32 - IDD Specification parameters and test conditions (VDD = 1.5V) 35
Table 33 - Electrical Characteristics and Recommended A.C. Operating Conditions 38
Table 34 - DDR3(L) Memory Components 44

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