June.2024

SCB13H4G160BF
SCB13H4G800BF

4Gbit DDR3L SDRAM
EU RoHS Compliant Products

Data Sheet

Rev. B

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2023-11	A	First version release
2024-6	B	1.Add Industrial temperature in Chapter 1 Features. 2.Add Industrial Temperature Range (-40°C- 95°C) in Table 1.

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Contents

1 Feature

- Power supply: VDD = VDDQ = 1.35V (1.283V - 1.45V)
- Backward compatible to VDD = VDDQ = 1.5V ± 0.075V
- Supports DDR3L devices to be backward compatible in 1.5V application
- Package: 96-Ball FBGA (x16) 78-Ball FBGA(x8)
- Array configuration: 8 Banks
- 8n-Bit prefetch architecture
- Differential clock inputs (CK, CK#)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- Average refresh period:
- -7.8us at 0℃ ≤ TCASE ≤ 85℃
- -3.9us at 85℃＜TCASE ≤ 95℃
- JEDEC JESD79-3F compliant
- RoHS complian
- Operating case temperature:
  -Commercial (0°C ≤ TC ≤ +95°C)
  -Industrial (-40°C ≤ TC ≤ +95°C)

Note:

1. The functionality described and the timing specifications included in this data sheet are for the DLL enabled mode of operation.

1.1 Product List

Table 1 shows all possible products within the 4Gbit DDR3L SDRAM component generation. Availability depends on application needs.

Table 1 - Ordering Information for4Gbit DDR3L Components

UniIC Part Number	Max. Clock frequency	Org	CAS-RCD-RP latencies	Speed Sort Name	Package
Commercial Temperature Range(0°C ~+95°C)					
SCB13H4G800BF-11M	933 MHz	× 8	13-13-13	DDR3L–1866M	PG-FBGA-78
SCB13H4G800BF-09N	1067 MHz	× 8	14-14-14	DDR3L–2133N	PG-FBGA-78
SCB13H4G160BF-11M	933 MHz	× 16	13-13-13	DDR3L–1866M	PG-FBGA-96
SCB13H4G160BF-09N	1067 MHz	× 16	14-14-14	DDR3L–2133N	PG-FBGA-96
Industrial Temperature Range (-40°C - 95°C)					
SCB13H4G800BF-11MI	933 MHz	X8	13-13-13	DDR3L–1866M	PG-FBGA-78
SCB13H4G800BF-09NI	1067 MHz	X8	14-14-14	DDR3L–2133N	PG-FBGA-78
SCB13H4G160BF-11MI	933 MHz	X16	13-13-13	DDR3L–1866M	PG-FBGA-96
SCB13H4G160BF-09NI	1067 MHz	X16	14-14-14	DDR3L–2133N	PG-FBGA-96

1.2 Address Table

Table 2 - Address Table

Parameter	512Mb x 8	256Mb x 16
Number of Banks	8	8
Bank Address	BA0 - BA2	BA0 - BA2
Auto Precharge	A10/AP	A10/AP
BC Switch on the fly	A12/BC#	A12/BC#
Row Address	A0 - A15	A0 - A14

Column Address	A0 - A9	A0 - A9
Page Size(1)	1KB	2KB

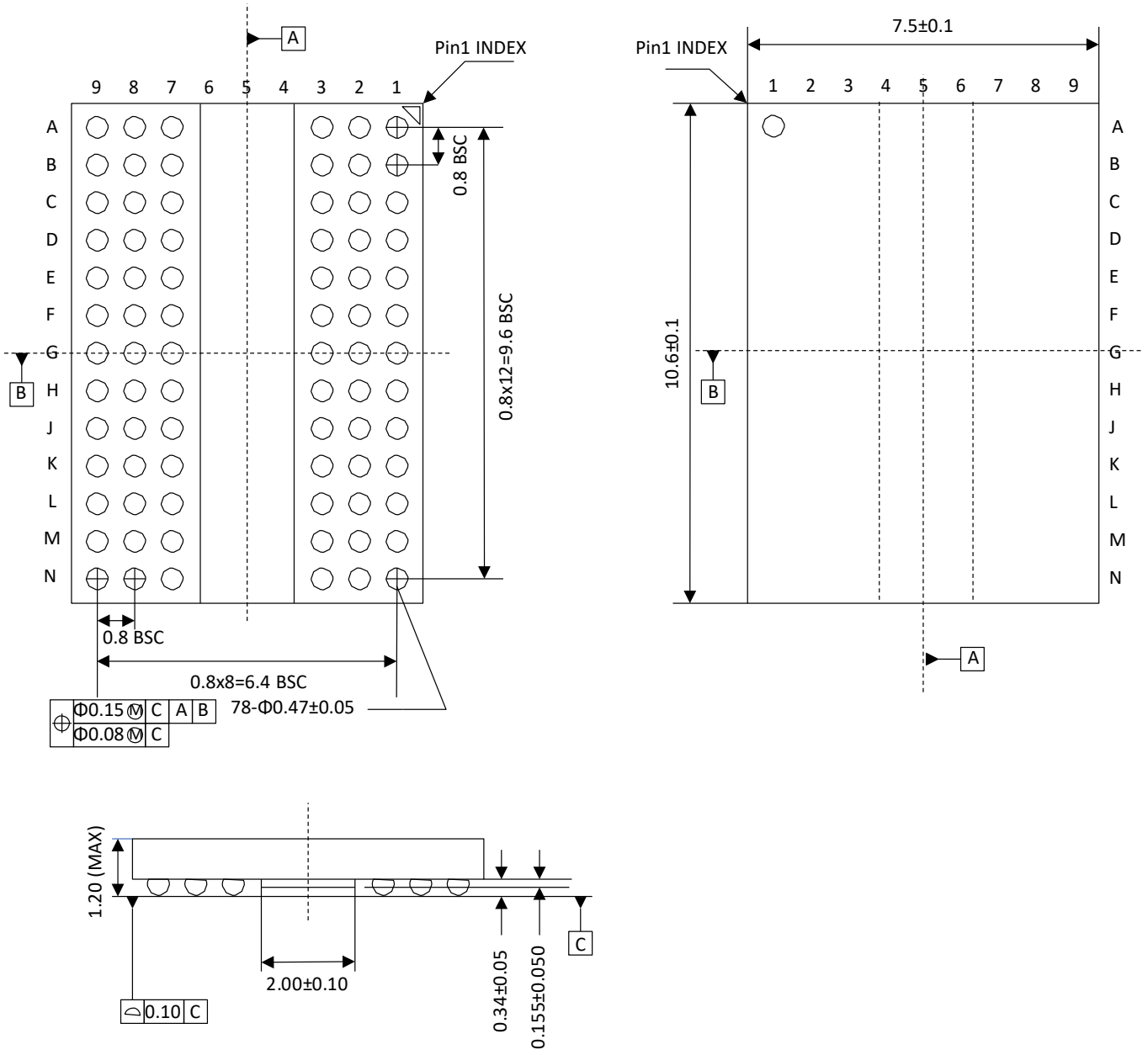
Note:

1. Page size is the number of bytes of the data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated asfollows:

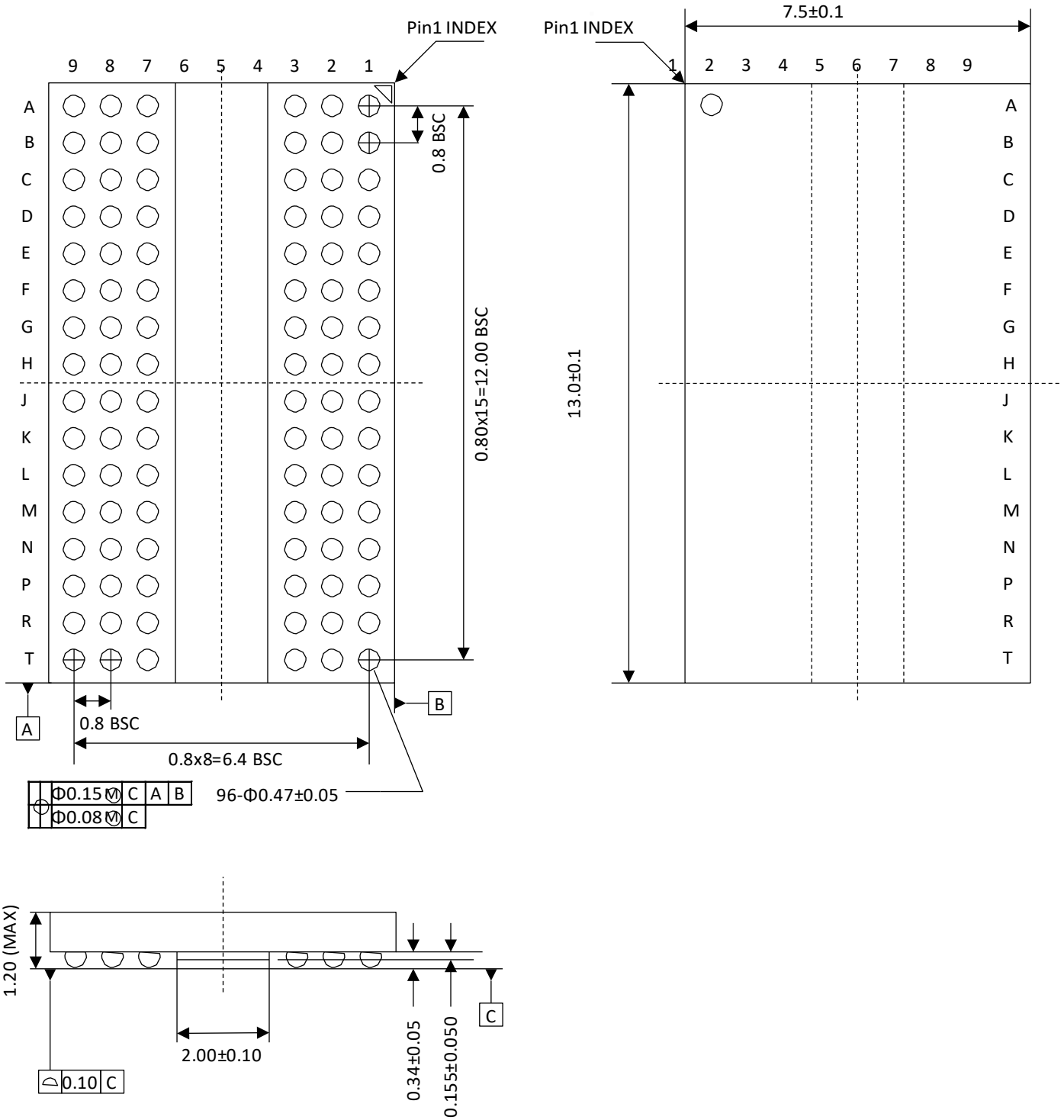
   Page size = $2^{COLBITS}$ × ORG / 8;
   COLBITS = the number of column address bits;ORG = the number of I/O (DQ) bits).

2 Package Information

2.1 Package 78-Ball FBGA (x8)



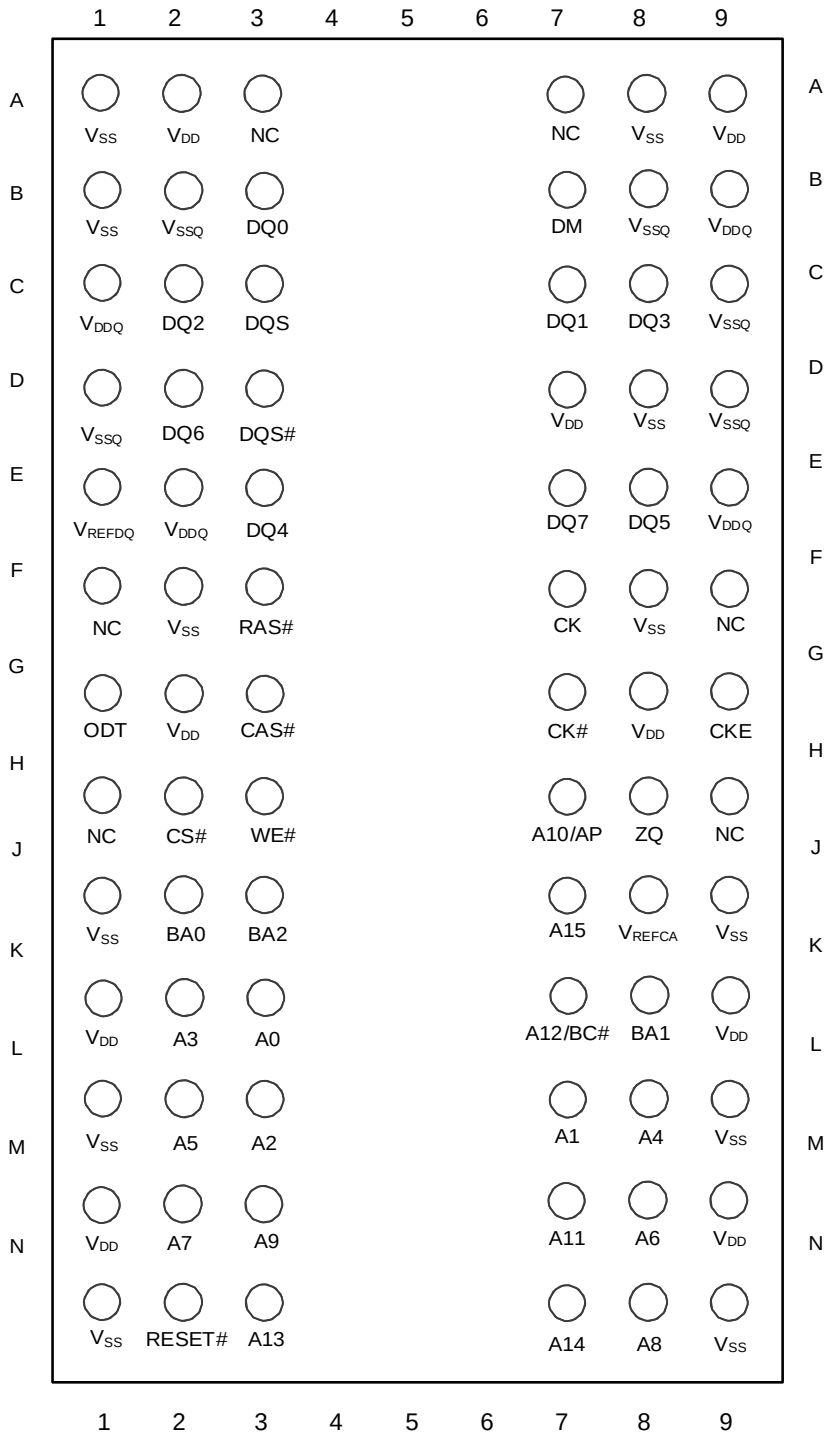
2.2 Package 96-Ball FBGA (x16)



3 Ball Assignments

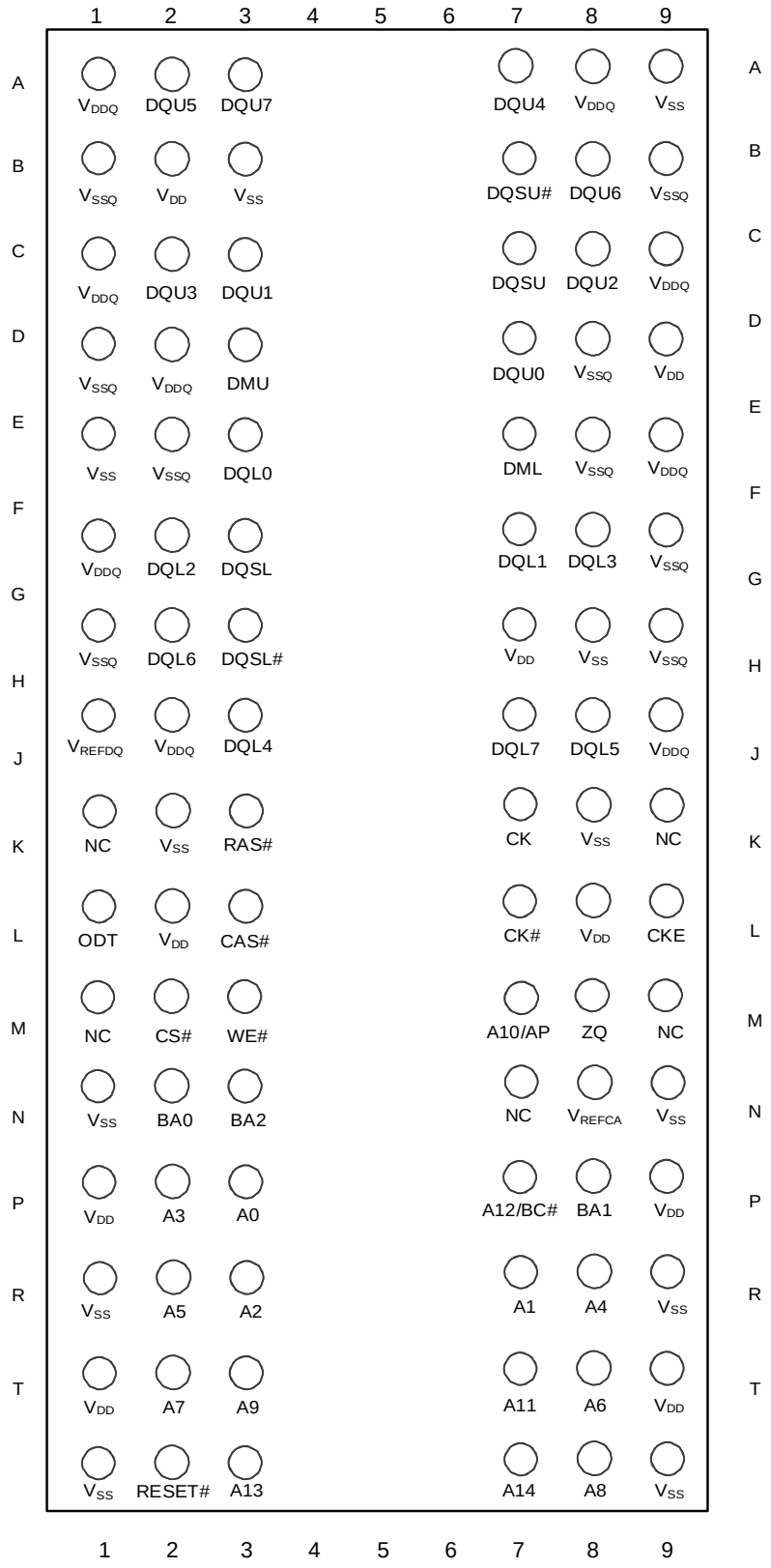
3.1 78- Ball FBGA (x8) Ball Assignments

Figure 1 – 78- Ball FBGA (x8) Ball Assignments



3.2 96-Ball FBGA (x16) Ball Assignments

Figure 2 - 96-Ball FBGA (x16) Ball Assignments



3.3 Ball Description

Table 3 - Ball Description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (read) data is referenced to the crossings of CK and CK#.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} and V_{REFDQ} have become stable during the power on and initialization sequence, they must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during SELF REFRESH.
CS#	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#, CAS# WE#	Input	Command Input: RAS#, CAS#, and WE# (along with CS#) defines the command being entered.
DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a write access. DM is sampled on both edges of DQS.
BA0 – BA2	Input	Bank Address Inputs: BA0 – BA2 define the bank to which an ACTIVE, READ, WRITE or PRECHARGE command is being applied. Bank address also determines which mode register is to be accessed during MRS cycle.
A0 – A15	Input	Address Inputs: Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions, see below). The address inputs also provide the op-code during MODE REGISTER SET commands.
A10/AP	Input	Auto Precharge: A10 is sampled during READ/WRITE commands to determine whether auto precharge should be performed to the accessed bank after the READ/WRITE operation. (HIGH: auto precharge; LOW: No auto precharge) A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/BC#	Input	Burst Chop: A12/BC# is sampled during READ/WRITE commands to determine if burst chop (on- the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped).

Symbol	Type	Function
RESET#	Input	Active LOW Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD, i.e., 1.2V for DC HIGH and 0.3V for DC LOW.
DQ DQL, DQU	I/O	Data Input/Output: Bi-directional data bus.
DQS, DQS# DQSL, DQSL# DQSU, DQSU#	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7, DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
NC	-	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: DDR3L operation = 1.283 to 1.450V; DDR3 operation = 1.425 to 1.575V.
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: DDR3L operation = 1.283 to 1.450V; DDR3 operation = 1.425 to 1.575V.
VSS	Supply	Ground
VREFDQ	Supply	Reference Voltage for DQ
VREFCA	Supply	Reference Voltage for CA
ZQ	Supply	Reference Pin for ZQ Calibration

Note: Input only pins (BA0 – BA2, A0 – A15, RAS#, CAS#, WE#, CS#, CKE, ODT and RESET#) do not supply termination.

4 Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

Figure 3 - 512 Meg x 8 Functional Block Diagram

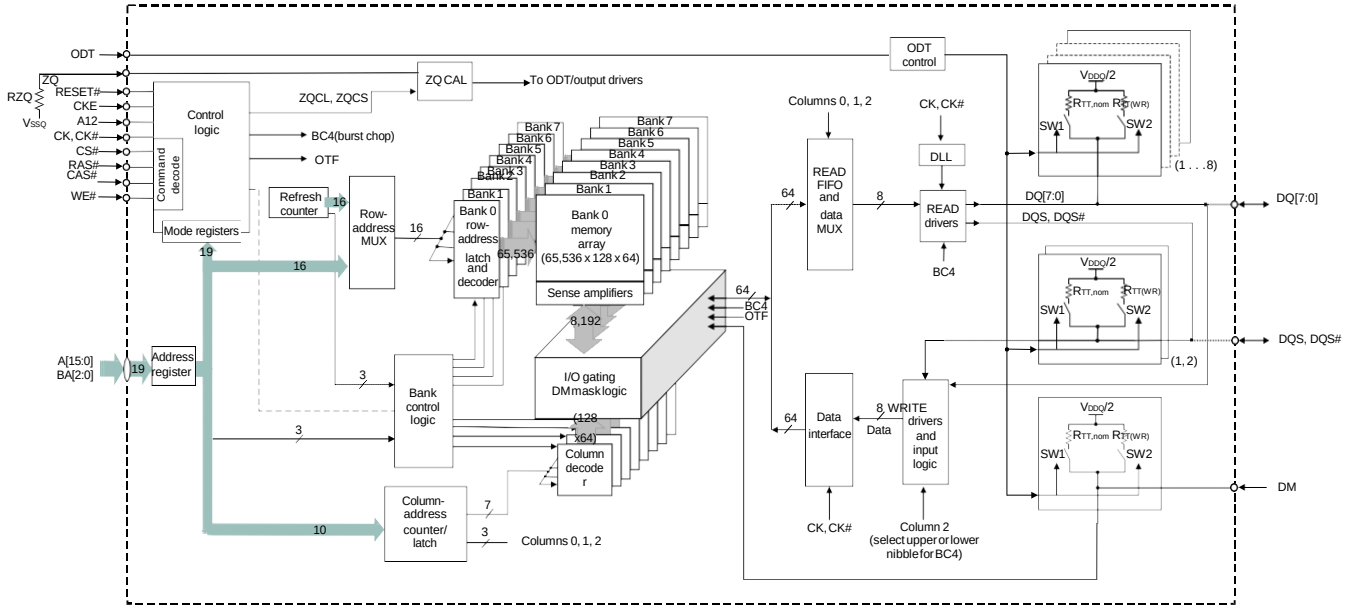
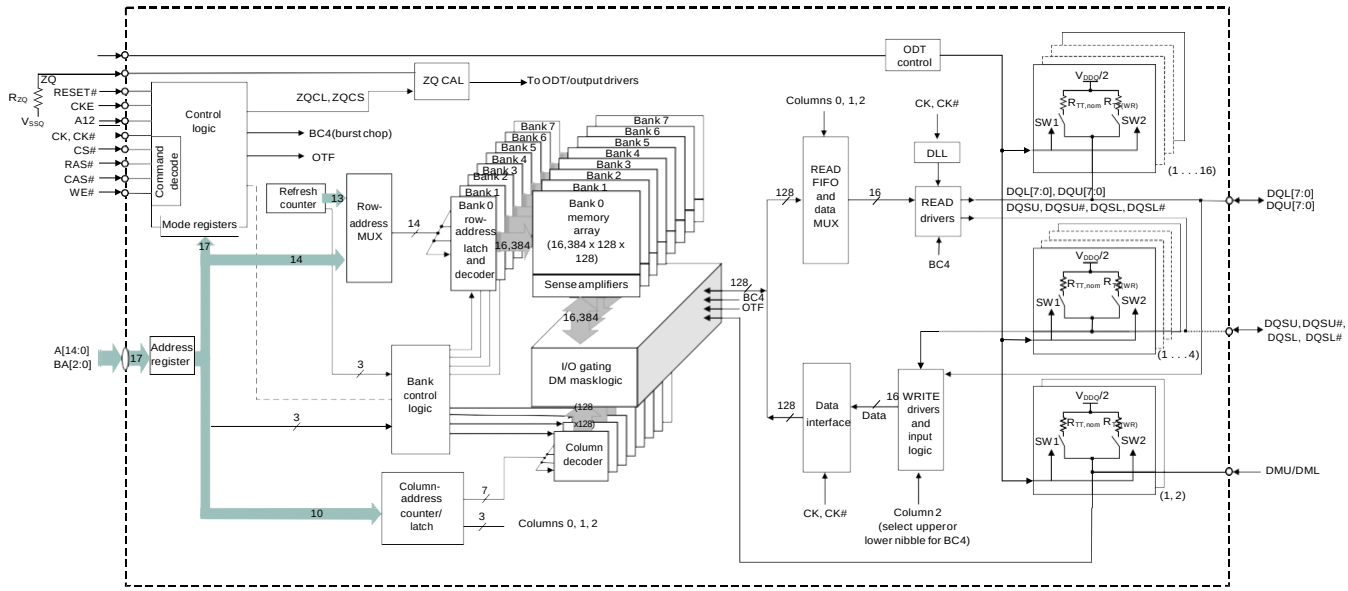


Figure 4 - 256 Meg x 16 Functional Block Diagram



5 Absolute Maximum Ratings

5.1 Absolute Maximum DC Ratings

Table 4 - Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Unit	Note
VDD	Voltage on VDD pin relative to VSS	-0.4 ~ 1.8	V	1,3
VDDQ	Voltage on VDDQ pin relative to VSS	-0.4 ~ 1.8	V	1,3
VIN, VOUT	Voltage on any pin relative to VSS	-0.4 ~ 1.8	V	1
TSTG	Storage Temperature	-55 ~ 100	°C	1,2

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD79-3F standard.
3. VDD and VDDQ must be within 300mV of each other at all times, and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV, VREF may be equal to or less than 300mV.

5.2 Recommended DC Operating Conditions

Table 5 - Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min	Typ.	Max		
V_{DD}	Supply voltage	DDR3L	1.283	1.35	1.45	V	1,2,3,4,5,6
		DDR3	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply voltage for output	DDR3L	1.283	1.35	1.45	V	1,2,3,4,5,6
		DDR3	1.425	1.5	1.575	V	1,2

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDD(t) over a long period of time (e.g., 1 sec).
4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
5. Under these supply voltages, the device operates to this DDR3L specification.
6. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.

5.3 DRAM Component Operating Temperature Range

Table 6 - Temperature Range

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Wide temperature	-40 ~ 85	°C	1,2
	Extended Temperature Range	85 ~ 95	°C	1,3

Note:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM. As for measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 ~ 85°C under all operating conditions.
3. Some applications require DRAM to operate in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   - REFRESH commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range.
   - If SELF REFRESH operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

6 AC And DC Input Measurement Levels

6.1 AC and DC Logic Input Levels for Single-ended Signals

6.1.1 AC and DC Input Levels for Single-ended Command and Address Signals

Table 7 - Single-ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866/2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
$V_{IH.CA(DC90)}$	DC input logic high	V_{REF}+0.09	V_{DD}	V_{REF} +0.09	V_{DD}	V_{REF} +0.09	V_{DD}	V	1
$V_{IL.CA(DC90)}$	DC input logic low	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V	1
$V_{IH.CA(AC160)}$	AC input logic high	V_{REF}+0.16	Note 2	V_{REF} +0.16	Note 2	-	-	V	1,2,5
$V_{IL.CA(AC160)}$	AC input logic low	Note 2	V_{REF} - 0.16	Note 2	V_{REF} - 0.16	-	-	V	1,2,5
$V_{IH.CA(AC135)}$	AC input logic high	V_{REF}+0.135	Note 2	V_{REF} +0.135	Note 2	V_{REF}+0.135	Note 2	V	1,2,5
$V_{IL.CA(AC135)}$	AC input logic low	Note 2	V_{REF} - 0.135	Note 2	V_{REF} - 0.135	Note 2	V_{REF} - 0.135	V	1,2,5
$V_{IH.CA(AC125)}$	AC input logic high	-	-	-	-	V_{REF}+0.125	Note 2	V	1,2,5
$V_{IL.CA(AC125)}$	AC input logic low	-	-	-	-	Note 2	V_{REF} - 0.125	V	1,2,5
$V_{REFCA(DC)}$	Reference voltage for ADD, CMD inputs	0.49 × V_{DD}	0.51 × V_{DD}	0.49 × V_{DD}	0.51 × V_{DD}	0.49 × V_{DD}	0.51 × V_{DD}	V	3,4

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		DDR3-1866/2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
$V_{IH.CA(DC100)}$	DC input logic high	V_{REF}+0.10	V_{DD}	V_{REF} +0.10	V_{DD}	V_{REF} + 0.10	V_{DD}	V	1,6
$V_{IL.CA(DC100)}$	DC input logic low	V_{SS}	V_{REF} - 0.10	V_{SS}	V_{REF} - 0.10	V_{SS}	V_{REF} - 0.10	V	1,7
$V_{IH.CA(AC175)}$	AC input logic high	V_{REF}+0.175	Note 2	V_{REF} +0.175	Note 2	-	-	V	1,2,8
$V_{IH.CA(AC175)}$	AC input logic low	Note 2	V_{REF} - 0.175	Note 2	V_{REF} - 0.175	-	-	V	1,2,9
$V_{IL.CA(AC150)}$	AC input logic high	V_{REF}+0.15	Note 2	V_{REF} +0.15	Note 2	-	-	V	1,2,8
$V_{IH.CA(AC150)}$	AC input logic low	Note 2	V_{REF} - 0.15	Note 2	V_{REF} - 0.15	-	-	V	1,2,9
$V_{IL.CA(AC135)}$	AC input logic high	-	-	-	-	V_{REF} + 0.135	Note 2	V	1,2,8
$V_{IH.CA(AC135)}$	AC input logic low	-	-	-	-	Note 2	V_{REF} -0.135	V	1,2,9
$V_{IL.CA(AC125)}$	AC input logic high	-	-	-	-	V_{REF} + 0.125	Note 2	V	1,2,8
$V_{IL.CA(AC125)}$	AC input logic low	-	-	-	-	Note 2	V_{REF} -0.125	V	1,2,9
$V_{REFCA(DC)}$	Reference voltage for ADD, CMD inputs	0.49 × V_{DD}	0.51 × V_{DD}	0.49 × V_{DD}	0.51 × V_{DD}	0.49 × V_{DD}	0.51 × V_{DD}	V	3,4,10

Note:

1. For input only pins except RESET#. $V_{REF} = V_{REFCA(DC)}$.
2. See “Overshoot and Undershoot Specifications” in Section 7.6.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF(DC)}$ by more than ± 1% V_{DD} (for reference: DDR3L: pprox.. ± 13.5mV; DDR3: pprox.. ±15mV).
4. For reference: DDR3 has pprox.. V_{DD}/2 ± 15mV, DDR3L has pprox.. V_{DD}/2 ± 13.5mV.
5. These levels apply for 1.35V operation only. If the device is operated at 1.5V, the respective levels in JESD79-3F ($V_{IH/L.CA(DC100)}$, $V_{IH/L.CA(AC175)}$, $V_{IH/L.CA(AC150)}$, $V_{IH/L.CA(AC135)}$, $V_{IH/L.CA(AC125)}$, etc.) apply. The 1.5V levels ($V_{IH/L.CA(DC100)}$, $V_{IH/L.CA(AC175)}$, $V_{IH/L.CA(AC150)}$, $V_{IH/L.CA(AC135)}$, $V_{IH/L.CA(AC125)}$, etc.) do not apply when the device is operated in the 1.35 voltage range.
6. $V_{IH(DC)}$ is used as a simplified symbol for $V_{IH.CA(DC100)}$.
7. $V_{IL(DC)}$ is used as a simplified symbol for $V_{IL.CA(DC100)}$.
8. $V_{IH(AC)}$ is used as a simplified symbol for $V_{IH.CA(AC175)}$, $V_{IH.CA(AC150)}$, $V_{IH.CA(AC135)}$, and $V_{IH.CA(AC125)}$; $V_{IH.CA(AC175)}$ value is used when V_{REF} + 0.175V is referenced, $V_{IH.CA(AC150)}$ value is used when V_{REF} + 0.15V is referenced, $V_{IH.CA(AC135)}$ value is used

when V_{REF} + 0.135V is referenced, and $V_{IH.CA(AC125)}$ value is used when V_{REF} + 0.125V is referenced.

9. $V_{IL(AC)}$ is used as a simplified symbol for $V_{IL.CA(AC175)}$, $V_{IL.CA(AC150)}$, $V_{IL.CA(AC135)}$ and $V_{IL.CA(AC125)}$; $V_{IL.CA(AC175)}$ value is used when V_{REF} – 0.175V is referenced, $V_{IL.CA(AC150)}$ value is used when V_{REF} – 0.15V is referenced, $V_{IL.CA(AC135)}$ value is used when V_{REF} – 0.135V is referenced, and $V_{IL.CA(AC125)}$ value is used when V_{REF} – 0.125V is referenced.
10. $V_{REFCA(DC)}$ is measured relative to V_{DD} at the same point in time on the same device.

6.1.2 AC and DC Input Levels for Single-ended Data Signals

Table 8 - Single-ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866/2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
$V_{IH.DQ(DC90)}$	DC input logic high	V_{REF}+0.09	V_{DD}	V_{REF}+0.09	V_{DD}	V_{REF}+0.09	V_{DD}	V	1
$V_{IL.DQ(DC90)}$	DC input logic low	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V	1
$V_{IH.DQ(AC160)}$	AC input logic high	V_{REF}+0.16	Note 2	-	-	-	-	V	1,2,5
$V_{IL.DQ(AC160)}$	AC input logic low	Note 2	V_{REF} – 0.16	-	-	-	-	V	1,2,5
$V_{IH.DQ(AC135)}$	AC input logic high	V_{REF}+0.135	Note 2	V_{REF}+0.135	Note 2	-	-	V	1,2,5
$V_{IL.DQ(AC135)}$	AC input logic low	Note 2	V_{REF} - 0.135	Note 2	V_{REF} - 0.135	-	-	V	1,2,5
$V_{IH.DQ(AC130)}$	AC input logic high	-	-	-	-	V_{REF}+0.13	Note 2	V	1,2,5
$V_{IL.DQ(AC130)}$	AC input logic low	-	-	-	-	Note 2	V_{REF} - 0.13	V	1,2,5
$V_{REFDQ(DC)}$	Reference voltage for DQ, DM inputs	0.49 × V_{DD}	0.51 × V_{DD}	0.49 × V_{DD}	0.51 × V_{DD}	0.49 × V_{DD}	0.51 × V_{DD}	V	3,4

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		DDR3-1866/2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
$V_{IH.DQ(DC100)}$	DC input logic high	V_{REF}+0.10	V_{DD}	V_{REF}+0.10	V_{DD}	V_{REF}+0.10	V_{DD}	V	1,6
$V_{IL.DQ(DC100)}$	DC input logic low	V_{SS}	V_{REF} - 0.10	V_{SS}	V_{REF} - 0.10	V_{SS}	V_{REF} - 0.10	V	1,7
$V_{IH.DQ(AC175)}$	AC input logic high	V_{REF}+0.175	Note 2	-	-	-	-	V	1,2,8
$V_{IL.DQ(AC175)}$	AC input logic low	Note 2	V_{REF} - 0.175	-	-	-	-	V	1,2,9
$V_{IH.DQ(AC150)}$	AC input logic high	V_{REF}+0.15	Note 2	V_{REF}+0.15	Note 2	-	-	V	1,2,8
$V_{IL.DQ(AC150)}$	AC input logic low	Note 2	V_{REF} – 0.15	Note 2	V_{REF} - 0.15	-	-	V	1,2,9
$V_{IH.DQ(AC135)}$	AC input logic high	V_{REF}+0.135	Note 2	V_{REF}+0.135	Note 2	V_{REF}+0.135	Note 2	V	1,2,8
$V_{IL.DQ(AC135)}$	AC input logic low	Note 2	V_{REF} - 0.135	Note 2	V_{REF} - 0.135	Note 2	V_{REF} - 0.135	V	1,2,9
$V_{REFDQ(DC)}$	Reference voltage for DQ, DM inputs	0.49 × V_{DD}	0.51 × V_{DD}	0.49 × V_{DD}	0.51 × V_{DD}	0.49 × V_{DD}	0.51 × V_{DD}	V	3,4,10

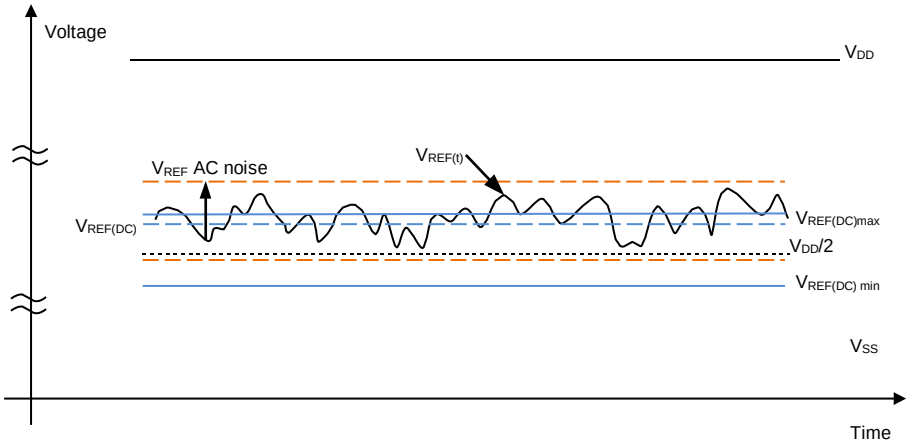
Note:

1. For input only pins except RESET#, VREF = VREFDQ(DC).
2. See “Overshoot and Undershoot Specifications” in Section 7.6.
3. The AC peak noise on VREF may not allow VREF to deviate from VREFDQ(DC) by more than ± 1% VDD (for reference: DDR3L:pprox.. ± 13.5mV; DDR3: pprox.. ± 15mV).
4. For reference: DDR3 has pprox.. VDD/2 ± 15mV, and DDR3L has pprox.. VDD/2 ± 13.5mV.
5. These levels apply for 1.35V operation only. If the device is operated at 1.5V, the respective levels in JESD79-3F (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135), etc.) apply. The 1.5V levels (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135), etc.) do not apply when the device is operated in the 1.35 voltage range.
6. VIH(DC) is used as a simplified symbol for VIH.DQ(DC100).
7. VIL(DC) is used as a simplified symbol for VIL.DQ(DC100).
8. VIH(AC) is used as a simplified symbol for VIH.DQ(AC175), VIH.DQ(AC150), and VIH.DQ(AC135); VIH.DQ(AC175) value is used when VREF + 0.175V is referenced, VIH.DQ(AC150) value is used when VREF + 0.15V is referenced, and VIH.DQ(AC135) value is used when VREF + 0.135V is referenced.
9. $V_{IL(AC)}$ is used as a simplified symbol for $V_{IL.DQ(AC175)}$, $V_{IL.DQ(AC150)}$, and $V_{IL.DQ(AC135)}$; $V_{IL.DQ(AC175)}$ value is used when VREF – 0.175V is referenced, VIL.DQ(AC150) value is used when VREF – 0.15V is referenced, and VIL.DQ(AC135) value is used when VREF – 0.135V is referenced.
10. $V_{REFDQ(DC)}$ is measured relative to V_{DD} at the same point in time on the same device.

6.2 V_{REF} Tolerances

The DC-Tolerance limits and AC-Noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrate in Figure 5. It shows a valid reference voltage $V_{REF(t)}$ as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).
$V_{REF(DC)}$ is the linear average of $V_{REF(t)}$ over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirement in Table 7. Furthermore $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than ± 1% VDD.

Figure 5 - Illustration of $V_{REF(DC)}$ Tolerance and V_{REF} AC-Noise limits

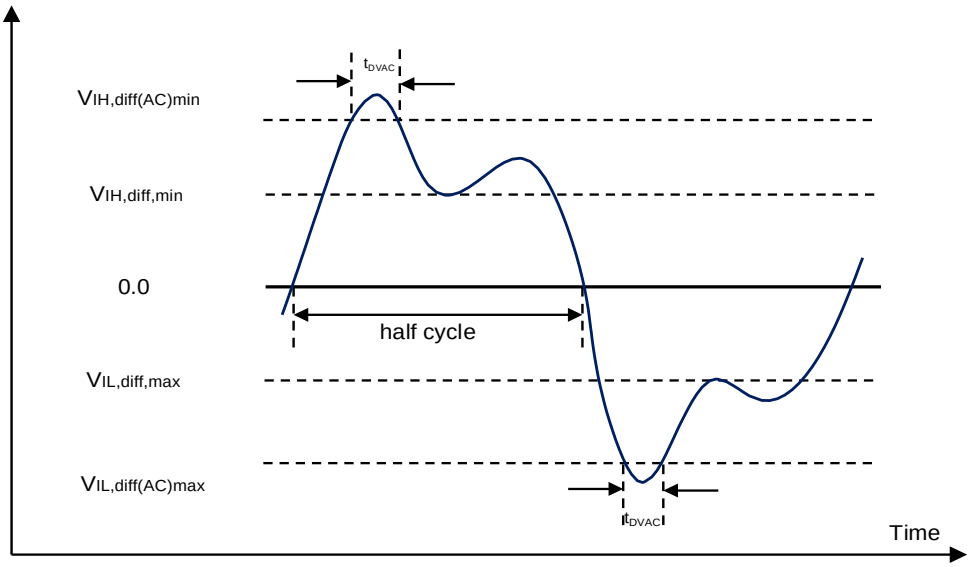


voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF. “VREF” should be understood as VREF(DC).
This clarifies that DC-Variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level, and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-Noise. Timing and voltage effects due to AC-Noise on VREF up to the specified limit (± 1% of VDD) are included in DRAM timings and their associated deratings.

6.3 AC and DC Logic Input Levels for Differential Signals

6.3.1 Differential Signals Definition

Figure 6 - Definition of Differential AC-Swing and “Time above AC-Level” t_{DVAC}



6.3.2 Diifferential Swing Requirements for Clock (CK – CK#) and strobe (DQS – DQS#)

Table 9 - Differential AC and DC Input Levels

Symbol	Parameter	DDR3L/DDR3-800/1066/1333/1600/1866				Unit	Note
		1.35V		1.5V			
		Min	Max	Min	Max		
$V_{IH,diff}$	Differential input high	+ 0.18	Note 3	+ 0.20	Note 3	V	1
$V_{IL,diff}$	Differential input low	Note 3	- 0.18	Note 3	- 0.20	V	1
$V_{IH,diff(AC)}$	Differential input high AC	2 x ($V_{IH(AC)}$ – V_{REF})	Note 3	2 x ($V_{IH(AC)}$ – V_{REF})	Note 3	V	2
$V_{IL,diff(AC)}$	Differential input low AC	Note 3	2 x ($V_{IL(AC)}$ – V_{REF})	Note 3	2 x ($V_{IL(AC)}$ – V_{REF})	V	2

Note:

1. Used to define a differential signal slew-rate.
2. For CK – CK# use VIH/VIL(AC) of ADD/CMD and VREFCA; for DQS – DQS#, DQSL – DQSL#, DQSU – DQSU# use VIH/VIL(AC) of DQS and VREFDQ; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however, the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 10 - Allowed Time before Ringback (t_{DVAC}) for CK – CK# and DQS – DQS# (1.35V)

Slew Rate [V/ns]	DDR3L-800/1066/1333/1600						DDR3L-1866/2133			
	t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = 320mV		t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = 270mV		t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = 270mV		t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = 250mV		t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = 260mV	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
>4.0	189	-	201	-	163	-	168	-	176	-
4.0	189	-	201	-	163	-	168	-	176	-
3.0	162	-	179	-	140	-	147	-	154	-
2.0	109	-	134	-	95	-	105	-	111	-
1.8	91	-	119	-	80	-	91	-	97	-
1.6	69	-	100	-	62	-	74	-	78	-
1.4	40	-	76	-	37	-	52	-	56	-
1.2	Note	-	44	-	5	-	22	-	24	-
1.0	Note	-	Note	-	Note	-	Note	-	Note	-
<1.0	Note	-	Note	-	Note	-	Note	-	Note	-

Note:

1. Rising input differential signal shall become equal to or greater than VIH,diff(AC) level and falling input signal shall become equal to or less than VIL,diff(AC) level.

Table 11 - Allowed Time before Ringback (t_{DVAC}) for CK – CK# and DQS – DQS# (1.5V)

Slew Rate [V/ns]	DDR3-800/1066/1333/1600						DDR3-1866/2133			
	t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = 350mV		t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = 300mV		t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = (DQS – DQS#) only		t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = 300mV		t_{DVAC} [ps] @ $V_{IH/L,diff(AC)}$ = (CK – CK#) only	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
>4.0	75	-	175	-	214	-	134	-	139	-
4.0	57	-	170	-	214	-	134	-	139	-
3.0	50	-	167	-	191	-	112	-	118	-
2.0	38	-	119	-	146	-	67	-	77	-
1.8	34	-	102	-	131	-	52	-	63	-
1.6	29	-	81	-	113	-	33	-	45	-
1.4	22	-	54	-	88	-	9	-	23	-
1.2	Note	-	19	-	56	-	Note	-	Note	-
1.0	Note	-	Note	-	11	-	Note	-	Note	-
<1.0	Note	-	Note	-	Note	-	Note	-	Note	-

Note:

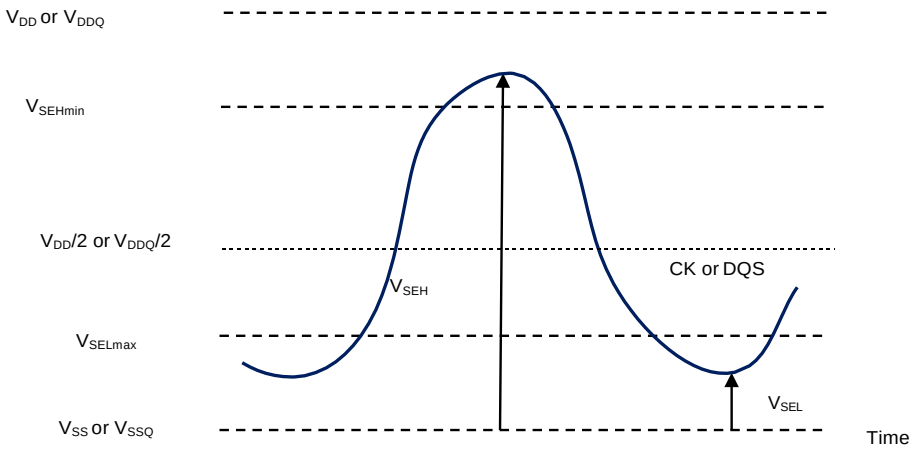
1. Rising input differential signal shall become equal to or greater than VIH,diff(AC) level and falling input differential signal shall become equal to or less than VIL,diff(AC) level.

6.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#) has also to comply with certain requirements for single-ended signals.
CK and CK# have to approximately reach VSEHmin/VSELmax (approximately equal to the AC-Levels (VIH(AC)/VIL(AC)) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, DQS#, DQSL# have to reach VSEHmin/VSELmax (approximately the AC-Levels (VIH(AC)/VIL(AC)) for DQ signal) in every half-cycle proceeding and following a valid transition.
Note that the applicable AC-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these AC-levels apply also for the single-ended signals CK and CK#.

Figure 7 - Single-ended Requirement for Differential Signals



Note that, while ADD/CMD and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDD/2, this is nominally the same. The transition of single-ended signals through the AC-Levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 12 - Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#

Symbol	Parameter	DDR3L/DDR3-800/1066/1333/1600/1866		Unit	Note
		Min	Max		
V_{SEH}	Single-ended high-level for strobes	(V_{DD}/2) + 0.175	Note 3	V	1,2
	Single-ended high-level for CK, CK#	(V_{DD}/2) + 0.175	Note 3	V	1,2
V_{SEL}	Single-ended low-level for strobes	Note 3	(V_{DD}/2) – 0.175	V	1,2
	Single-ended low-level for CK, CK#	Note 3	(V_{DD}/2) – 0.175	V	1,2

Note:
1. For CK, CK# use VIH/VIL(AC) of ADD/CMD; for storbes (DQS, DQS#, DQSL, DQSL#, DQSU, DQSU#) use VIH/VIL(AC) of DQS.
2. VIH(AC)/VIL(AC) for DQ is based on VREFDQ; VIH(AC)/VIL(AC) for ADD/CMD is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

6.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table 13 and Table 14. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

Figure 8 - V_{IX} Definition

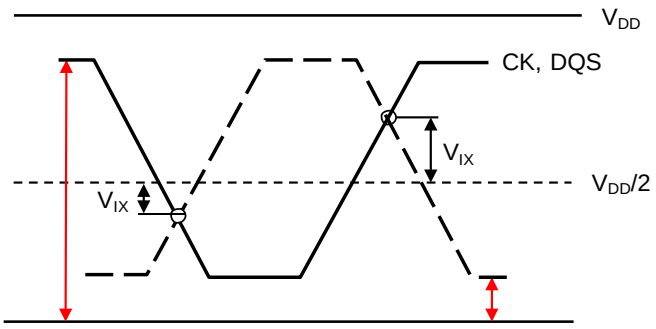


Table 13 - Cross Point Voltage for Differential Input Signals (CK, DQS):1.35V

Symbol	Parameter	DDR3L-800/1066/1333/1600/1866/2133		Unit	Note
		Min	Max		
$V_{IX(CK)}$	Differential Input Cross Point Voltage relative to V_{DD}/2 for CK, CK#	-150	150	mV	1
$V_{IX(DQS)}$	Differential Input Cross Point Voltage relative to V_{DD}/2 for DQS, DQS#	-150	150	mV	-

Note:

1. The relation between VIX(min/max) and VSEL/VSEH should satisfy following.
   (VDD/2) + VIX(min) – VSEL ≥ 25mV;
   VSEH – ((VDD/2) + VIX(max)) ≥ 25mV.

Table 14 - Cross Point Voltage for Differential Input Signals (CK, DQS):1.5V

Symbol	Parameter	DDR3-800/1066/1333/1600/1866/2133		Unit	Note
		Min	Max		
$V_{IX(CK)}$	nput Cross Point Voltage relative to V_{DD}/2 for CK, CK#	-150	150	mV	2
		-175	175	mV	1
$V_{IX(DQS)}$	Differential Input Cross Point Voltage relative to V_{DD}/2 for DQS, DQS#	-150	150	mV	2

Note:

1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing V_{SEL}/V_{SEH} of at least $V_{DD/2}$ ± 250mV, and when the differential slew rate of CK – CK# is larger than 3V/ns.
2. The relation between $VIX_{(min/max)}$ and V_{SEL}/V_{SEH} should satisfy following.
   ($V_{DD/2}$) + $VIX_{(min)}$ – V_{SE}L ≥ 25mV; V_{SEH} – (($V_{DD/2}$) + $V_{IX(max)}$) ≥ 25mV.

6.5 Slew Rate Definitions for Single-ended Input Signals

See section 11.5 “Address/Command Setup, Hold and Derating” single-ended slew rate definitions for address and command signals.
See section 11.6 “Data Setup, Hold and Slew Rate Derating” single-ended slew rate definitions for data signals.

6.6 Slew Rate Definitions for Differential Input Signals

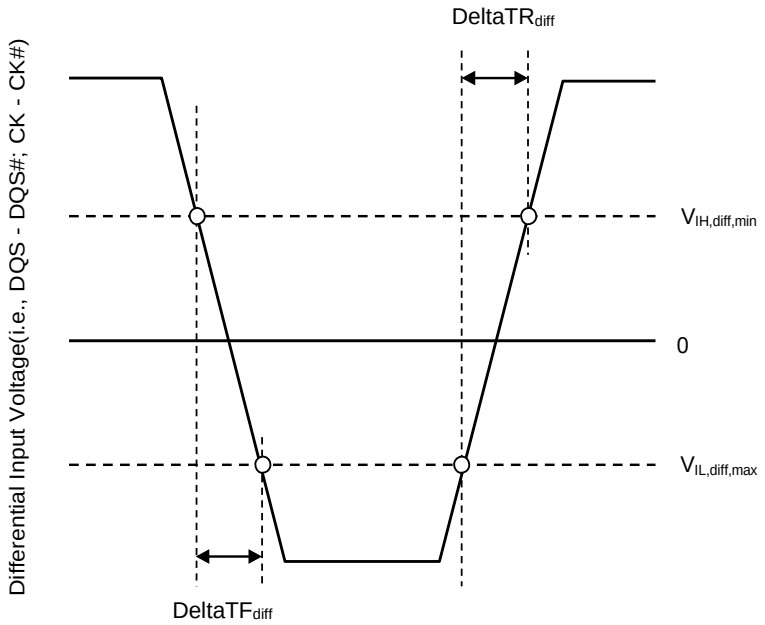
Input slew rate for differential signals (CK, CK#, and DQS, DQS#) are defined and measured as shown in Table15 and Figure 9.

Table 15 - Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK – CK# and DQS – DQS#)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$[V_{IH,diff,min} – V_{IL,diff,max}]/DeltaTR_{diff}$
Differential input slew rate for falling edge (CK – CK# and DQS – DQS#)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$[V_{IH,diff,min} – V_{IL,diff,max}]/DeltaTF_{diff}$

Note:
1. The differential signal (i.e., CK – CK# and DQS – DQS#) must be linear between these thresholds.

Figure 9 - Differentia l Input Slew Rate Definition for DQS, DQS# and CK, CK#



7 AC&DC Output Measurement Levels

7.1 Single-ended AC and DC Output Levels

Table 15 shows the output levels used for measurements of single-ended signals.

Table 16 - Single-ended AC&DC Output Levels

Symbol	Parameter	Value	Unit	Note
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	-
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	-
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	-
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} – 0.1 x V_{DDQ}	V	1

Note:
1. The swing of ± 0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2.

7.2 Differential AC and DC Output Levels

Table 16 shows the output levels used for measurements of differential signals.

Table 17 - Differential AC&DC Output Levels

Symbol	Parameter	Value	Unit	Note
$V_{OH,diff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OL,diff(AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	1

Note:

1. The swing of ± 0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

7.3 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single-ended signals as shown in Table 18 and Figure 10.

Table 18 - Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} – V_{OL(AC)}]$/DeltaTR$_{se}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} – V_{OL(AC)}]$/DeltaTF$_{se}$

Note:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure 10 - Single-ended Output Slew Rate Definition

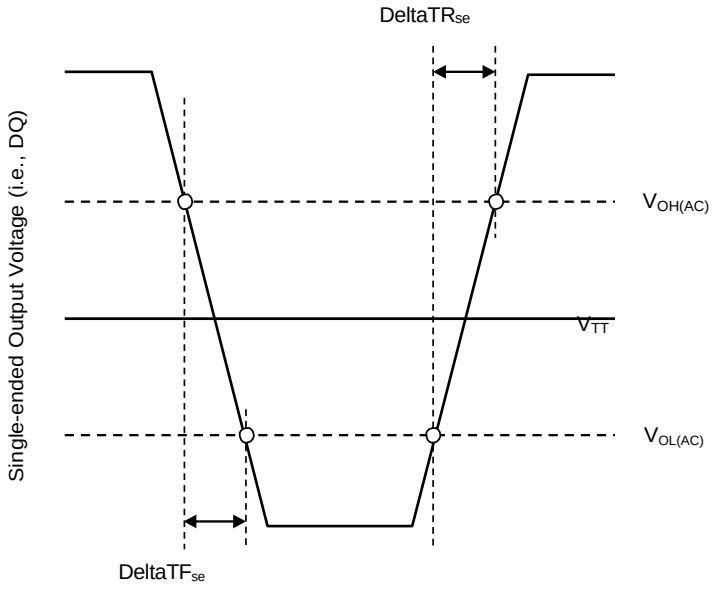


Table 19 - Single-ended Output Slew Rate

Parameter	Symbol	Operation Voltage	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		DDR3L-2133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
single-ended output slew rate	SRQ_{se}	1.35V	1.75	5(1)	1.75	5(1)	1.75	5(1)	1.75	5(1)	1.75	5(1)	1.75	5(1)	V/ns
		1.5V	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5(1)	2.5	5(1)	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Singnals

For RON = RZQ/7 Setting

Note:

1. In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.
   - Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from HIGH to LOW or LOW to HIGH) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either HIGH or LOW).
   - Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from HIGH to LOW or LOW to HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from LOW to HIGH or HIGH to LOW respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5V/ns applies).

7.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL,diff(AC) and VOH,diff(AC) for differential signals as shown in Table 20 and Figure 11.

Table 20 - Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/DeltaTR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/DeltaTF_{diff}$

Note:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure 11 - Differential Output Slew Rate Definition

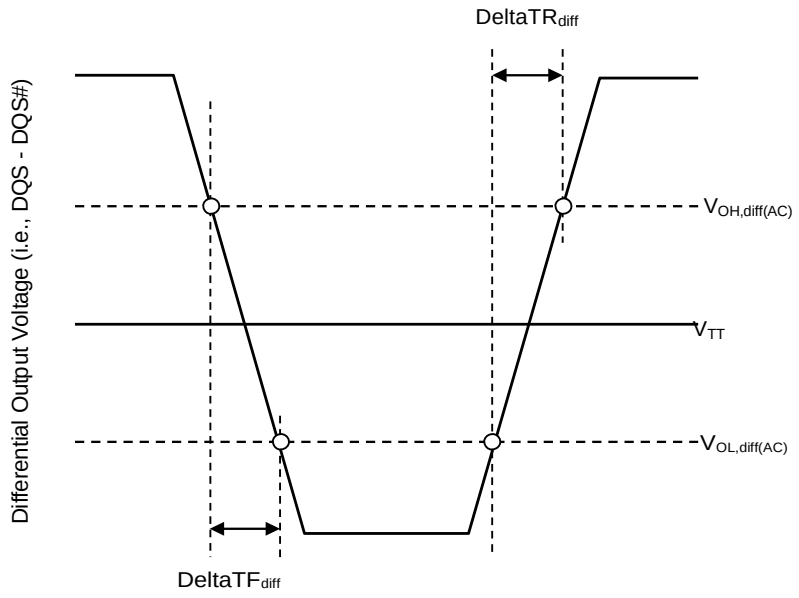


Table 21 - Differential Output Slew Rate

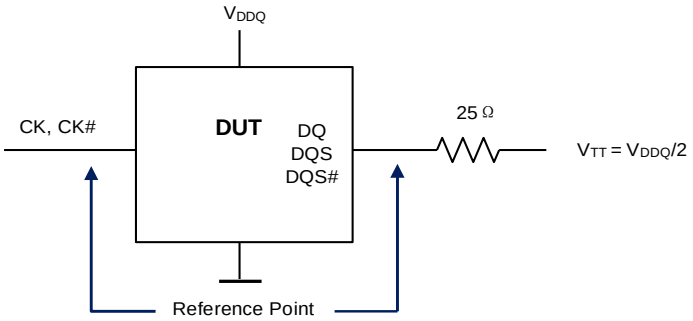
Parameter	Symbol	Operation Voltage	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		DDR3L-2133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
single-ended output slew rate	SRQ_{diff}	1.35V	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	V/ns
		1.5V	5	10	5	10	5	10	5	10	5	12	5	12	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
Diff: Differential Singnals
For $R_{ON} = R_{ZQ}/7$ Setting

7.5 Reference Load for AC Timing and Output Slew Rate

Figure 13 represents the effective reference load of 25Ω used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.
It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 12 - Reference Load for AC Timing and Output Slew Rate



7.6 Overshoot and Undershoot Specifications

7.6.1 Address and Control Overshoot and Undershoot Specifications

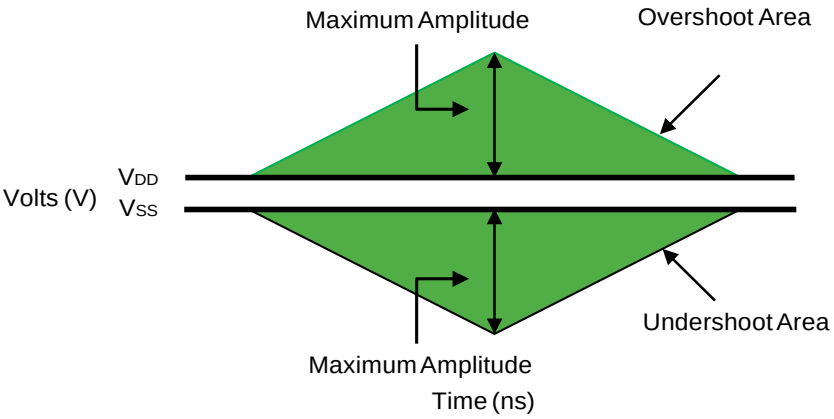
Table 22 - AC Overshoot/Undershoot Specification for Address and Control Pins

	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	Unit
Maximum peak amplitude allowed for overshoot area(1)	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area(2)	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD	0.67	0.5	0.4	0.33	0.28	0.25	V-ns
Maximum undershoot area below VSS	0.67	0.5	0.4	0.33	0.28	0.25	V-ns
(A0 – A15, BA0 – BA2, CS#, RAS#, CAS#, WE#, CKE, ODT)							

Note:

1. The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of the applied voltage (V_{DD}) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.

Figure 13 - Address and Control Overshoot and Undershoot Definition



7.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

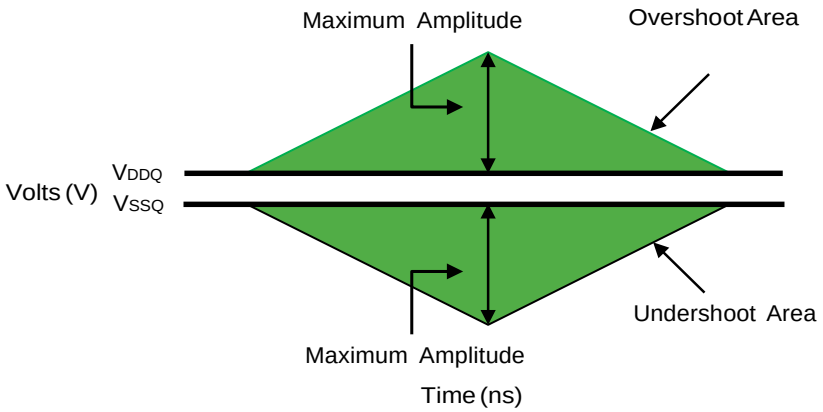
Table 23 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

	800	1066	1333	1600	1866	2133	Unit
Maximum peak amplitude allowed for overshoot area(1)	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area(2)	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDDQ	0.25	0.19	0.15	0.13	0.11	0.10	V-ns
Maximum undershoot area below VSSQ	0.25	0.19	0.15	0.13	0.11	0.10	V-ns
(CK, CK#, DQ, DQS, DQS#, DM)							

Note:

1. The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of the applied voltage (VDD) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.

Figure 14 - Clock, Data, Strobe and Mask Overshoot and Undershoot Definition



7.7 34Ω Output Driver DC Electronic Characteristics

A functional representation of the output buffer is shown below. Output driver impedance RON is defined by the value of external reference resistor RZQ as follows:
RON34 = RZQ/7 (Nominal 34.3Ω ± 10% with nominal RZQ = 240Ω).
The individual pull-up and pull-down resistors RON(Pu) and RON(Pd) are defined as follows:

under the condition that RON(Pd) is turned off .
under the condition that RON(Pu) is turned off.

Figure 15 - Output Driver: Definition of Voltages and Currents

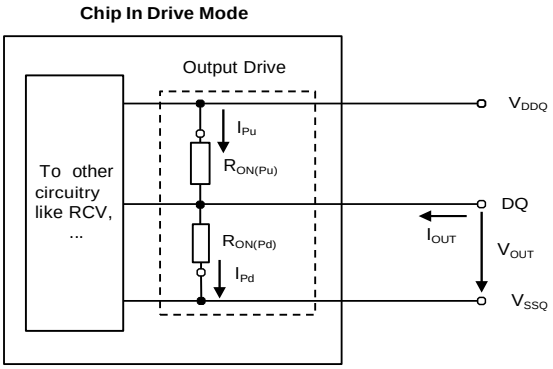


Table 24 - Output Driver DC Electrical Characteristics, assuming RZQ = 240Ω; entire operating temperature range; after proper ZQ calibration

RON,Nom	Resistor	VOUT	Min	Nom	Max (DDR3L)	Max (DDR3)	Unit	Note
34Ω	$R_{ON,34Pd}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/7$	1,2,3
		$V_{OM(DC)}$ = 0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/7$	1,2,3
		$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/7$	1,2,3
	$R_{ON,34Pu}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/7$	1,2,3
		$V_{OM(DC)}$ = 0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/7$	1,2,3
		$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/7$	1,2,3
40Ω	$R_{ON,40Pd}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3
		$V_{OM(DC)}$ = 0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3
		$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/6$	1,2,3
	$R_{ON,40Pu}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/6$	1,2,3
		$V_{OM(DC)}$ = 0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3
		$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3
Mismatch between pull-up and pull-down, MM_{PuPd}		$V_{OM(DC)}$ = 0.5 x V_{DDQ}	-10	-	+10	+10	%	1,2,4

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd: Measure RON(Pu) and RON(Pd), both at 0.5 × VDDQ:

7.7.1 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 25 and Table 26
$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@calibration)$; $V_{DD} = V_{DDQ}$.

Note:

1. $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

Table 25 - Output Driver Sensitivity Denfinition

Item	Min	Max	Unit
$R_{ON(Pu)}@V_{OH(DC)}$	0.6 – $dR_{ON}dTH \times \lvert\Delta T\rvert$ - $dR_{ON}dVH \times \lvert\Delta V\rvert$	1.1 + $dR_{ON}dTH \times \lvert\Delta T\rvert$ + $dR_{ON}dVH \times \lvert\Delta V\rvert$	$R_{ZQ}/7$
$R_{ON}@V_{OM(DC)}$	0.9 – $dR_{ON}dTM \times \lvert\Delta T\rvert$ - $dR_{ON}dVM \times \lvert\Delta V\rvert$	1.1 + $dR_{ON}dTM \times \lvert\Delta T\rvert$ + $dR_{ON}dVM \times \lvert\Delta V\rvert$	$R_{ZQ}/7$
$R_{ON(Pd)}@V_{OL(DC)}$	0.6 – $dR_{ON}dTL \times \lvert\Delta T\rvert$ - $dR_{ON}dVL \times \lvert\Delta V\rvert$	1.1 + $dR_{ON}dTL \times \lvert\Delta T\rvert$ + $dR_{ON}dVL \times \lvert\Delta V\rvert$	$R_{ZQ}/7$

Table 26 - Output Driver Voltage and Temperature Sensitivity

Speed Bin	800/1066/1333		1600/1866/2133		Unit
Item	Min	Max	Min	Max	
$dR_{ON}dTM$	0	1.5	0	1.5	%/℃
$dR_{ON}dVM$	0	0.15	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	0	1.5	%/℃
$dR_{ON}dVL$	0	0.15	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	0	1.5	%/℃
$dR_{ON}dVH$	0	0.15	0	0.13	%/mV

Note:

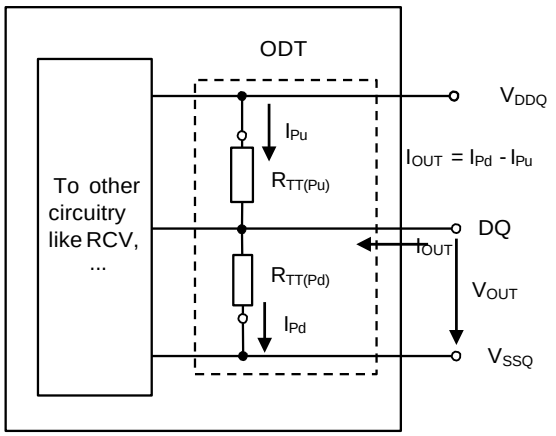
1. These parameters may not be subject to production test. They are verified by design and characterization.

7.8 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of MR1 register. ODT is applied to the DQ, DM, DQS/DQS# pins.
A functional representation of the on-die termination is shown below. The individual pull-up and pull-down resistors (RTT(Pu) and RTT(Pd)) are defined as follows:
Under the condition that RTT(Pd) is turned off.
Under the condition that RTT(Pu) is turned off.

Figure 16 - On-Die Termination: Definition of Voltages and Currents

Chip In Termination Mode



ODT DC Electrical Characteristic

Table 27 provides an overview of the ODT DC electrical characteristics. Their values for RTT60(Pd120), RTT60(Pu120), RTT120(Pd240), RTT120(Pu240), RTT40(Pd80), RTT40(Pu80), RTT30(Pd60), RTT30(Pu60), RTT20(Pd40), RTT20(Pu40) are not specification requirements, but can be used as design guide lines.

Table 27 - ODT DC Electristics, assuming R_{ZQ} = 240Ω ± 1% entire operating temperature range; after proper ZQ calibration

MR1 (A9, A6, A2)	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max (DDR3L)	Max (DDR3)	Unit	Note
(0,1,0)	120Ω	$R_{TT120(Pd240)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	R_{ZQ}	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	R_{ZQ}	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	R_{ZQ}	1,2,3,4
		$R_{TT120(Pu240)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	R_{ZQ}	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	R_{ZQ}	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	R_{ZQ}	1,2,3,4
		R_{TT120}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/2$	1,2,5
(0,0,1)	60Ω	$R_{TT60(Pd120)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/2$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/2$	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/2$	1,2,3,4
		$R_{TT60(Pu120)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/2$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/2$	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/2$	1,2,3,4
		R_{TT60}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/4$	1,2,5
(0,1,1)	40Ω	$R_{TT40(Pd80)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/3$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/3$	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/3$	1,2,3,4
		$R_{TT40(Pu80)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/3$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/3$	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/3$	1,2,3,4
		R_{TT40}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/6$	1,2,5
(1,0,1)	30Ω	$R_{TT30(Pd60)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/4$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/4$	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/4$	1,2,3,4
		$R_{TT30(Pu60)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/4$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/4$	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/4$	1,2,3,4
		R_{TT30}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/8$	1,2,5
(1,0,0)	20Ω	$R_{TT20(Pd40)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/6$	1,2,3,4
		$R_{TT20(Pu40)}$	$V_{OL(DC)}$ = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/6$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3,4
			$V_{OH(DC)}$ = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3,4
		R_{TT20}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/12$	1,2,5
Deviation of V_M w.r.t $V_{DDQ}/2$, ΔVM Deviation of V_M w.r.t $V_{DDQ}/2$, ΔVM				-5	-	+5	+5	%	1,2,5,6

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for RTT:
   Apply VIH(AC) to pin under test and measure current I(VIH(AC)), then apply VIL(AC) to pin under test and measure current I(VIL(AC)) respectively.

$$R_{TT} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

6. Measurement definition for VM and ΔVM: Δmeasure voltage (VM) at test pin (midpoint) with no load:

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1 \right) \times 100$$

7.8.1 ODT DC Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 28 and Table 29.

$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@calibration)$; $V_{DD} = V_{DDQ}$.

Table 28 - ODT Sensitivity Definition

	Min	Max	Unit
R_{TT}	$0.9 - dR_{TT}dT \times \lvert\Delta T\rvert - dR_{TT}dV \times \lvert\Delta V\rvert$	$1.6 + dR_{TT}dT \times \lvert\Delta T\rvert + dR_{TT}dV \times \lvert\Delta V\rvert$	R_{ZQ}/2,4,6,8,12

Table 29 - ODT Voltage and Temperature Sensitivity

	Min	Max	Unit
$dR_{TT}dT$	0	1.5	%/℃
$dR_{TT}dV$	0	0.15	%/mV

Note:

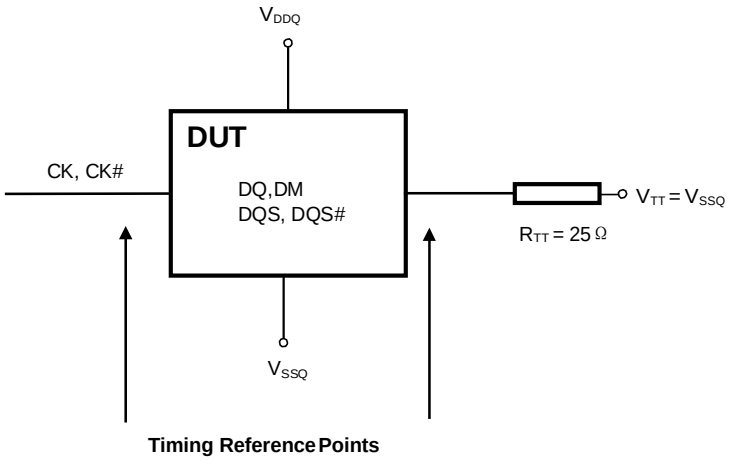
1. These parameters may not be subject to production test. They are verified by design and characterization.

7.9 ODT Timing Definitions

7.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 17.

Figure 17 - ODT Timing Reference Load



7.9.2 ODT Timing Definitions

Definitions for tAON, tAONPD, tAOF, tAOFPD and tADC are provided in Table 30 and subsequent figures. Measurement reference settings are provided in Table 31

Table 30 - ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK – CK# defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	Figure 18
t_{AONPD}	Rising edge of CK – CK# with ODT being first registered HIGH	Extrapolated point at V_{SSQ}	Figure 19
t_{AOF}	Rising edge of CK – CK# defined by the end point of ODTLoff	End point: Extrapolated point at $V_{RTT,Nom}$	Figure 20
t_{AOFPD}	Rising edge of CK – CK# with ODT being first registered LOW	End point: Extrapolated point at $V_{RTT,Nom}$	Figure 21
t_{ADC}	Rising edge of CK – CK# defined by the end point of ODTLcnw, ODTLcwn4 of ODTLcwn8	End point: Extrapolated points at $V_{RTT(WR)}$ and $V_{RTT,Nom}$ respectively	Figure 22

Table 31 - ODT Timing Definitions

Measured Parameter		$R_{TT,Nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}[V]	V_{SW2}[V]
t_{AON}		$R_{ZQ}/4$	NA	0.05	0.10
		$R_{ZQ}/12$	NA	0.10	0.20
t_{AONPD}		$R_{ZQ}/4$	NA	0.05	0.10
		$R_{ZQ}/12$	NA	0.10	0.20
t_{AOF}		$R_{ZQ}/4$	NA	0.05	0.10
		$R_{ZQ}/12$	NA	0.10	0.20
t_{AOFPD}		$R_{ZQ}/4$	NA	0.05	0.10
		$R_{ZQ}/12$	NA	0.10	0.20
t_{ADC}	DDR3L(1.35V)	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.25
	DDR3(1.5V)	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.30

Figure 18 - Definition of t_{AON}

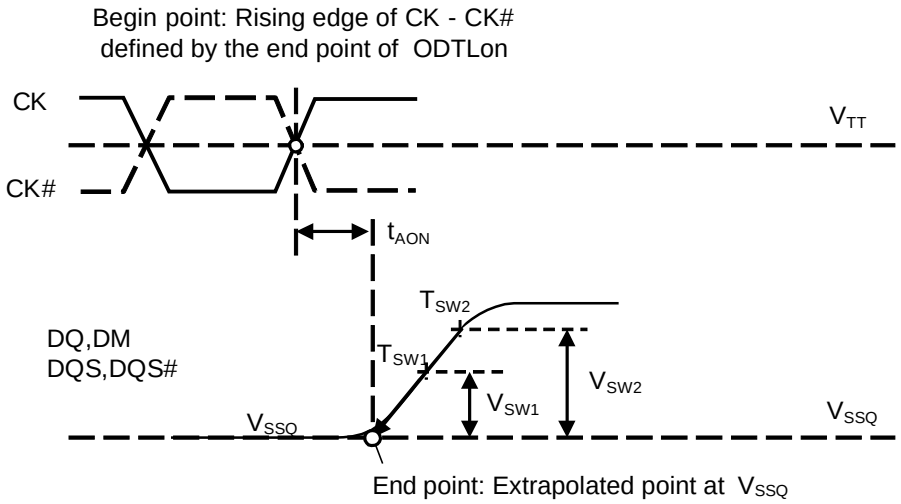


Figure 19 - Definition of tAONPD

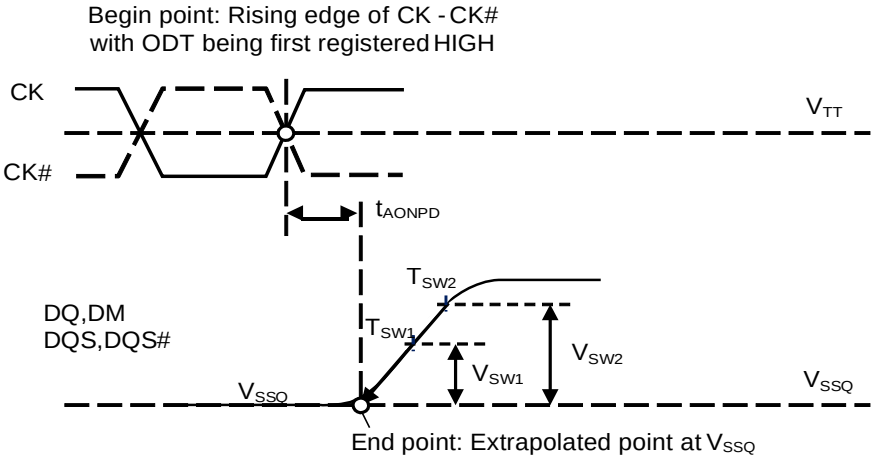


Figure 20 - Definition of t_{AOF}

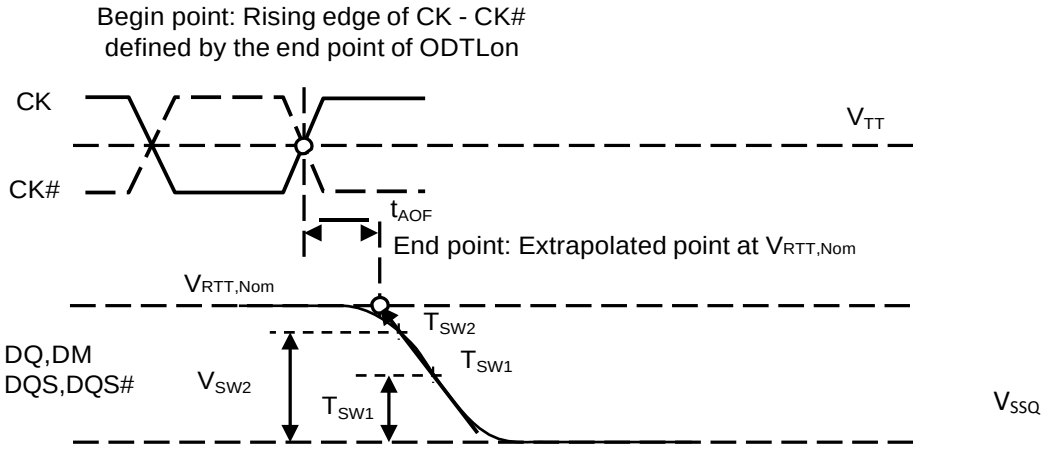


Figure 21 - Definition of t_{AOFPD}

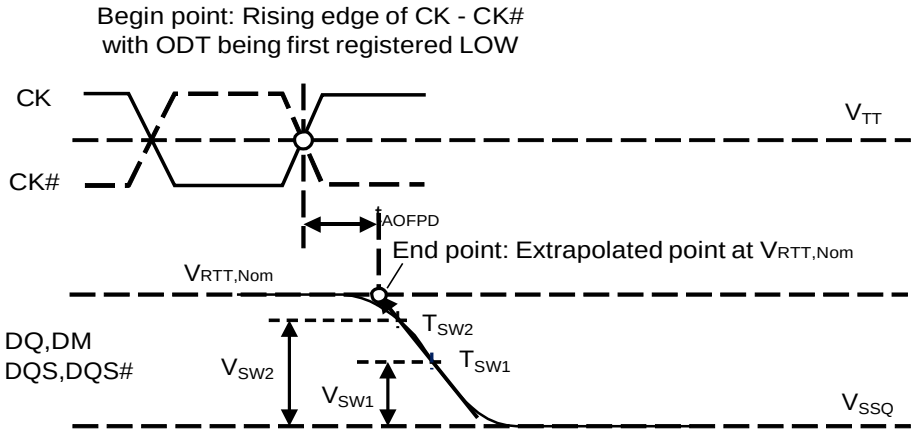
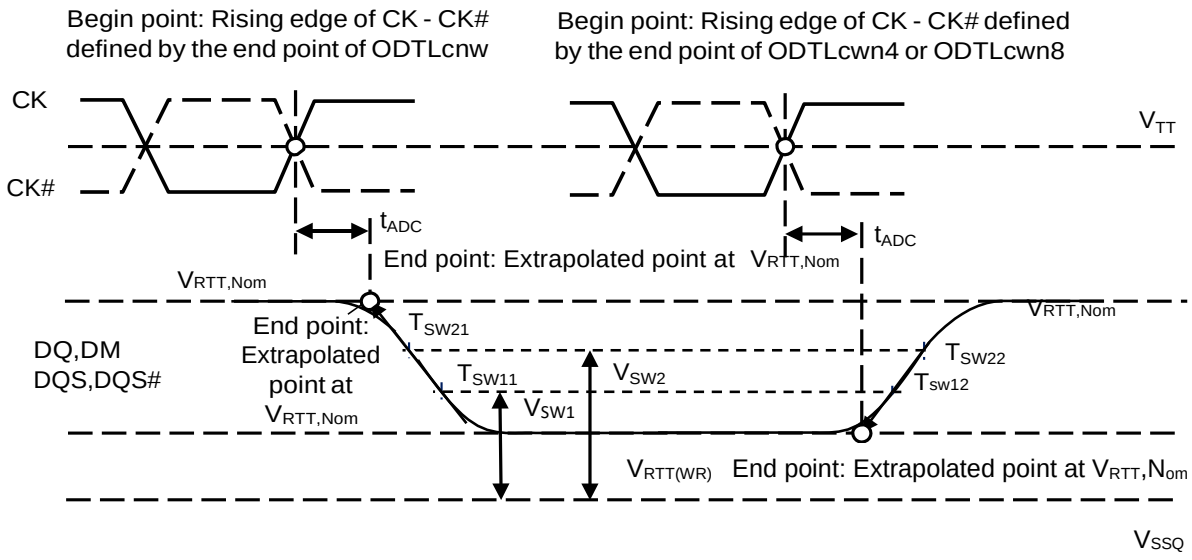


Figure 22 - Definition of t_{ADC}



8 I_{DD} Current Measure Method

8.1 I_{DD} Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.
Figure 23 shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in Figure 24. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN ≤ VIL.AC(max).

- "1" and "HIGH" is defined as VIN ≥ VIH.AC(min).
- "FLOATING" is defined as inputs are VREF = VDD/ 2.
- "Timing used for IDD and IDDQ Measured – Loop Patterns" are provided in Table 32.
- "Basic IDD and IDDQ Measurement Conditions" are described in Table 33.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 34 through Table 41.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting: RON = RZQ/7 (34Ω in MR1)
  Qoff = 0b (Output Buffer enabled in MR1)
  RTT,Nom = RZQ/6 (40Ω in MR1)
  RTT(WR) = RZQ/2 (120Ω in MR2)

Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Define D = {CS#, RAS#, CAS#, WE#} = {HIGH, LOW, LOW, LOW}
- Define D# = {CS#, RAS#, CAS#, WE#} = {HIGH, HIGH, HIGH, HIGH}

Figure 23 - Measurement Setup and Test Load for I_{DD} and I_{DDQ} Measurements

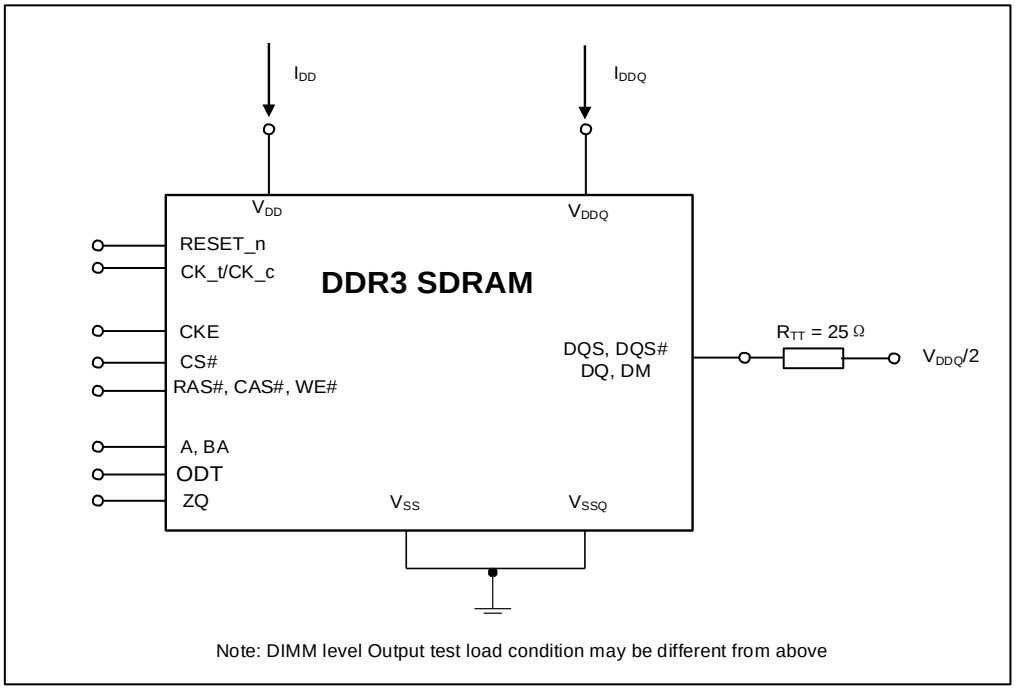


Figure 24 - Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by I_{DDQ} Measurement

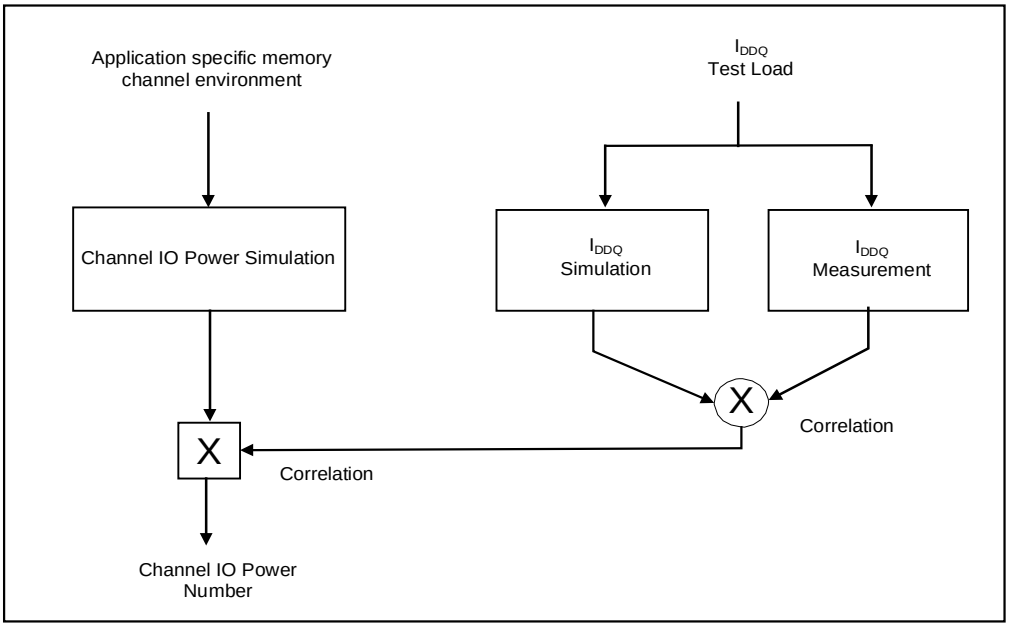


Table 32 - Timing used for I_{DD} and I_{DDQ} Measured-Loop Patterns for 1866/2133

Symbol		DDR3/DDR3L 1866	DDR3/DDR3L 2133	Unit
		13-13-13	14-14-14	
t_{CK}		1.071	0.938	ns
CL		13	14	nCK
nRCD		13	14	nCK
nRC		45	50	nCK
nRAS		32	36	nCK
nRP		13	14	nCK
nFAW	1KB page size	26	27	nCK
	2KB page size	33	38	nCK
nRRD	1KB page size	5	6	nCK
	2KB page size	6	7	nCK
nRFC 512Mb		85	97	nCK
nRFC 1Gb		103	118	nCK
nRFC 2Gb		150	172	nCK
nRFC 4Gb		243	279	nCK
nRFC 8Gb		328	375	nCK

Table 33 - Basic I_{DD} and I_{DDQ} Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: HIGH External Clock: On t_{CK}, nRC, nRAS, nRCD, CL: See Table 33 BL: 8(1) AL: 0 CS#: HIGH between ACT and PRE Command, Address, Bank Address Inputs: Partially toggling according to Table 34 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2, ... (see Table 34) Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0 Pattern Details: See Table 34.
I_{DD1}	Operating One Bank Active-Read-Precharge Current CKE: HIGH External Clock: On t_{CK}, nRC, nRAS, nRCD, CL: See Table 33 BL: 8(1,7) AL: 0 CS#: HIGH between ACT, RD and PRE Command, Address, Bank Address Inputs, Data I/O: Partially toggling according to Table 35 DM: Stable at 0 Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2, … (see Table 35) Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0 Pattern Details: See Table 35
I_{DD2N}	Precharge Standby Current CKE: HIGH External Clock: On t_{CK}, CL: See Table 33 BL: 8(1) AL: 0 CS#: Stable at 1 Command, Address, Bank Address Inputs: Partially toggling according to Table 36 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: All banks closed Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0 Pattern Details: See Table 36
I_{DD2NT}	Precharge Standby ODT Current CKE: HIGH External Clock: On t_{CK}, CL: See Table 33 BL: 8(1) AL: 0 CS#: Stable at 1 Command, Address, Bank Address Inputs: Partially toggling according to Table 37 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: All banks closed Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Toggling according to Table 37 Pattern Details: Table 37
I_{DDQ2NT}	Precharge Standby ODT I_{DDQ} Current Same definition like for I_{DD2NT}, however measuring I_{DDQ} current instead of I_{DD} current.

Symbol	Description
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: LOW External Clock: On t_{CK}, CL: See Table 33 BL: 8(1) AL: 0 CS#: Stable at 1 Command, Address, Bank Address Inputs: Stable at 0 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: All banks closed Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0 Pecharge Power Down Mode: Slow Exit(3)
I_{PP2P1}	Precharge Power-Down Current Fast Exit CKE: LOW External Clock: On t_{CK}, CL: See Table 33 BL: 8(1) AL: 0 CS#: Stable at 1 Command, Address, Bank Address Inputs: Stable at 0 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: All banks closed Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0
I_{DD2Q}	Precharge Quiet Standby Current CKE: HIGH External Clock: On t_{CK}, CL: See Table 33 BL: 8(1) AL: 0 CS#: Stable at 1 Command, Address, Bank Address Inputs: Stable at 0 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: All banks closed Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0
I_{DD3N}	Active Standby Current CKE: HIGH External Clock: On t_{CK}, CL: See Table 33 BL: 8(1) AL: 0 CS#: Stable at 1 Command, Address, Bank Address Inputs: Partially toggling according to Table 36 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: All banks open Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0 Pattern Details: See Table 36
I_{DD3P}	Active Power-Down Current CKE: LOW External Clock: On t_{CK}, CL: See Table 33 BL: 8(1) AL: 0 CS#: Stable at 1 Command, Address, Bank Address Inputs: Stable at 0 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: All banks open Output Buffer and R_{TT}: Enabled in Mode Registers(2)

Symbol	Description
I_{DD4R}	Operating Burst Read Current CKE: HIGH External Clock: On t_{CK}, CL: See Table 33 BL: 8(1,7) AL: 0 CS#: HIGH between RD7 Command, Address, Bank Address Inputs: Partially toggling according to Table 38 Data I/O: Seamless read data burst with different data between one burst and the next one according to Table 38 DM: Stable at 0 Bank Activity: All banks open, RD commands cycling through banks: 0,0,1,1,2,2, ... (see Table 38) Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0 Pattern Details: See Table 38
I_{DDQ4R}	Operating Burst Read I_{DDQ} Current Same definition like for I_{DD4R}, however measuring I_{DDQ} current instead of I_{DD} current.
I_{DD4W}	Operating Burst Write Current CKE: HIGH External Clock: On t_{CK}, CL: See Table 33 BL: 8(1) AL: 0 CS#: HIGH between WR Command, Address, Bank Address Inputs: Partially toggling according to Table 39 Data I/O: Seamless write data burst with different data between one burst and the next one according to Table 39 DM: Stable at 0 Bank Activity: All banks open, WR commands cycling through banks: 0,0,1,1,2,2, ... (see Table 39) Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at HIGH Pattern Details: See Table 39
I_{DD5B}	Burst Refresh Current CKE: HIGH External Clock: On t_{CK}, CL nRFC: See Table 33 BL: 8(1) AL: 0 CS#: HIGH between REF Command, Address, Bank Address Inputs: Partially toggling according to Table 40 Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: REF command every nRFC (see Table 40) Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0 Pattern Details: See Table 40
I_{DD6}	Self Refresh Current: Normal Temperature Range T_{CASE}: 0 – 85°C Auto Self Refresh (ASR): Disabled(4) Self Refresh Temperature Range (SRT): Normal(5) CKE: LOW External Clock: Off CK and CK#: LOW CL: See Table 33 BL: 8(1) AL: 0 CS#, Command, Address, Bank Address, Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: Self Refresh operation Output Buffer and R_{TT}: Enabled in Mode Registers(2)

Symbol	Description
I_{DD6ET}	Self Refresh Current: Extended Temperature Range T_{CASE}: 0 – 95°C Auto Self Refresh (ASR): Disabled(4) Self Refresh Temperature Range (SRT): Extended(5) CKE: LOW External Clock: Off CK and CK#: LOW CL: See Table 33 BL: 8(1) AL: 0 CS#, Command, Address, Bank Address, Data I/O: MID-LEVEL DM: Stable at 0 Bank Activity: Extended Temperature Self Refresh operation Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: MID-LEVEL
I_{DD7}	Operating Bank Interleave Read Current CKE: HIGH External Clock: On t_{CK}, nRC, nRAS, nRCD, nRRD, nFAW, CL: See Table 33 BL: 8(1) AL: CL-1 CS#: HIGH between ACT and RDA Command, Address, Bank Address Inputs: Partially toggling according to Table 41 Data I/O: Read data bursts with different data between one burst and the next one according to Table 41 DM: Stable at 0 Bank Activity: Two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 41 Output Buffer and R_{TT}: Enabled in Mode Registers(2) ODT Signal: Stable at 0 Pattern Details: See Table 41
I_{DD8}	RESET Low Current RESET: LOW External Clock: Off CK and CK#: LOW CKE: FLOATING CS#, Command, Address, Bank Address, Data I/O: FLOATING ODT Signal: FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.

Note:

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0] = 00b.
2. Output Buffer Enable: Set MR1 A[12] = 0b; set MR1 A[5,1] = 01b.
   RTT,Nom enable: Set MR1 A[9,6,2] = 011b.
   RTT(WR) enable: Set MR2 A[10,9] = 10b.
3. Pecharge Power Down Mode: Set MR0 A12 = 0b for Slow Exit or MR0 A12 = 1b for Fast Exit.
4. Auto Self Refresh (ASR): Set MR2 A6 = 0b to disable or 1b to enable feature.
5. Self Refresh Temperature Range (SRT): Set MR2 A7 = 0b for normal or 1b for extended temperature range.
6. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0b.

Table 34 - I_{DD0} Measurement-Loop Pattern(1)

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data(2)
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1…4 until nRAS – 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			…	repeat pattern 1…4 until nRC – 1, truncate if necessary												
			1 × nRC + 0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1 × nRC + 1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1 × nRC + 3,4	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
			…	repeat pattern nRC + 1…4 until 1 × nRC + nRAS – 1, truncate if necessary												
			1 × nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			…	repeat nRC + 1…4 until 2 × nRC – 1, truncate if necessary												
		1	2 × nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4 × nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6 × nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8 × nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10 × nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12 × nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14 × nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

Note:
1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 35 - I_{DD1} Measurement-Loop Pattern(1)

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data(2)
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1…4 until nRCD – 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			…	repeat pattern 1…4 until nRAS – 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			…	repeat pattern 1…4 until nRC – 1, truncate if necessary												
			1 × nRC + 0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1 × nRC + 1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1 × nRC + 3,4	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
			…	repeat pattern nRC + 1…4 until nRC + nRCD – 1, truncate if necessary												
			1 × nRC + nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			…	repeat pattern nRC + 1…4 until nRC + nRAS – 1, truncate if necessary												

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
			1 × nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			…	repeat pattern nRC + 1…4 until 2 × nRC – 1, truncate if necessary												
		1	2 × nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4 × nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6 × nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8 × nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10 × nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12 × nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14 × nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by READ Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 36 - I_{DD2N} and I_{DD3N} Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	D#	1	1	1	1	0	0	0	0	0	F	0	-
			3	D#	1	1	1	1	0	0	0	0	0	F	0	-
		1	4 – 7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8 – 11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12 – 15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16 – 19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20 – 23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24 – 27	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28 – 31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 37 - I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	D#	1	1	1	1	0	0	0	0	0	F	0	-
			3	D#	1	1	1	1	0	0	0	0	0	F	0	-
		1	4 – 7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8 – 11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12 – 15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16 – 19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20 – 23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24 – 27	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28 – 31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 38 - I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static HIGH	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
		1	8 – 15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16 – 23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24 – 31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32 – 39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40 – 47	repeat Sub-Loop 0, cbut BA[2:0] = 5												
		6	48 – 55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56 – 63	repeat Sub-Loop 0, but BA[2:0] = 7												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by READ Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 39 - I_{DD4W} Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static HIGH	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	D#, D#	1	1	1	1	1	0	00	0	0	F	0	-
		1	8 – 15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16 – 23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24 – 31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32 – 39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40 – 47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48 – 55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56 – 63	repeat Sub-Loop 0, but BA[2:0] = 7												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are used according to WR Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by WRITE Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 40 - I_{DD5B} Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static HIGH	0	0	REF	0	0	0	1	0	0	00	0	0	0	0	-
		1	1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
			5 – 8	repeat cycles 1 – 4, but BA[2:0] = 1												
			9 – 12	repeat cycles 1 – 4, but BA[2:0] = 2												
			13 – 16	repeat cycles 1 – 4, but BA[2:0] = 3												
			17 – 20	repeat cycles 1 – 4, but BA[2:0] = 4												
			21 – 24	repeat cycles 1 – 4, but BA[2:0] = 5												
			25 – 28	repeat cycles 1 – 4, but BA[2:0] = 6												
			29 – 32	repeat cycles 1 – 4, but BA[2:0] = 7												
		2	33 – nRFC – 1	repeat Sub-Loop 1, until nRFC – 1. Truncate, if necessary.												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 41 - I_{DD7} Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static HIGH		0	ACT	0	0	1	1	0	0	0	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	0
			2	D	1	0	0	0	0	0	0	0	0	0	0	-
		0	…	repeat above D Command until nRRD – 1												
			nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	-
			nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	110011
			nRRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	-
		1	…	repeat above D Command until 2 x nRRD – 1												
		2	2 × nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3 × nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4 × nRRD	D	1	0	0	0	0	3	0	0	0	F	0	-
				assert and repeat above D Command until nFAW – 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW + nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW + 2 × nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW + 3 × nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9		D	1	0	0	0	0	7	0	0	0	F	0	-
			nFAW + 4 × nRRD	assert and repeat above D Command until 2 × nFAW – 1, if necessary												
		10	2 × nFAW + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	-
			2 × nFAW + 1	RDA	0	1	0	1	0	0	0	1	0	F	0	110011
				D	1	0	0	0	0	0	0	0	0	F	0	-
			2 × nFAW + 2	repeat above D Command until 2 × nFAW + nRRD – 1												
		11	2 × nFAW + nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	-
			2 × nFAW + nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	0
				D	1	0	0	0	0	1	0	0	0	0	0	-
			2 × nFAW + nRRD + 2	repeat above D Command until 2 × nFAW + 2 × nRRD – 1												
		12	2 × nFAW + 2 × nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2 × nFAW + 3 × nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												

CK, CK#	CKE	Sub-Loop	Cycle	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data(2)
Toggling	Static HIGH	14	2 × nFAW + 4 × nRRD	D	1	0	0	0	0	3	0	0	0	0	0	-
				assert and repeat above D Command until 3 × nFAW – 1, if necessary												
		15	3 × nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3 × nFAW + nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3 × nFAW + 2 × nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3 × nFAW + 3 × nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3 × nFAW + 4 × nRRD	D	1	0	0	0	0	7	0	0	0	0	0	-
				assert and repeat above D Command until 4 × nFAW – 1, if necessary												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by READ Command. Outside burst operation, DQ signals are MID-LEVEL.

8.2 I_{DD} Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

Table 42 – I_{DD} Specifications (1.35V)

Speed Grade Bin	DDR3L-1866	DDR3L-2133	Unit	Notes
Symbol	Max.	Max.		
I_{DD0}	tbd	tbd	mA	x8
	78	83	mA	x16
I_{DD1}	tbd	tbd	mA	x8
	111	116	mA	x16
$I_{DD2P(0)}$ slow exit	36	39	mA	x8/x16
$I_{DD2P(1)}$ fast exit	37	40	mA	x8/x16
I_{DD2N}	59	64	mA	x8/x16
I_{DD2NT}	tbd	tbd	mA	x8
	85	89	mA	x16
I_{DD2Q}	49	53	mA	x8/x16
I_{DD3P} fast exit	67	70	mA	x8/x16
I_{DD3N}	tbd	tbd	mA	x8
	92	96	mA	x16
I_{DD4R}	tbd	tbd	mA	x8
	243	265	mA	x16
I_{DD4W}	tbd	tbd	mA	x8
	245	264	mA	x16
I_{DD5B}	292	294	mA	x8/x16
I_{DD6}	31	32	mA	x8/x16
I_{DD6ET}(1)	47	47	mA	x8/x16
I_{DD6TC}	46	47	mA	x8/x16
I_{DD7}	tbd	tbd	mA	x8
	269	272	mA	x16
I_{DD8}	tbd	tbd	mA	x8
	19	19	mA	x16

Note:

1. Applicable for MR2 setting A6 = 0b and A7 = 0b. Temperature range for IDD6 is 0 – 85°C at commercial temperature, -40 – 85°C at industrial temperature.
2. Applicable for MR2 setting A6 = 0b and A7 = 1b. Temperature range for IDD6ET is 0 – 95°C at commercial temperature & industrial temperature.
3. Some data retains the possibility of future updates.

Table 43 - I_{DD} Specifications (1.5V)

Speed Grade Bin	DDR3-1866	DDR3-2133	Unit	Notes
Symbol	Max.	Max.		
I_{DD0}	tbd	tbd	mA	x8
	85	90	mA	x16
I_{DD1}	tbd	tbd	mA	x8
	119	125	mA	x16
$I_{DD2P(0)}$ slow exit	40	43	mA	x8/x16
$I_{DD2P(1)}$ fast exit	40	43	mA	x8/x16
I_{DD2N}	62	65	mA	x8/x16
I_{DD2NT}	tbd	tbd	mA	x8
	90	94	mA	x16
I_{DD2Q}	55	59	mA	x8/x16
I_{DD3P} fast exit	68	71	mA	x8/x16
I_{DD3N}	tbd	tbd	mA	x8
	95	98	mA	x16
I_{DD4R}	tbd	tbd	mA	x8
	269	292	mA	x16
I_{DD4W}	tbd	tbd	mA	x8
	269	289	mA	x16
I_{DD5B}	317	318	mA	x8/x16
I_{DD6}	32	32	mA	x8/x16
I_{DD6ET}[1]	47	47	mA	x8/x16
I_{DD6TC}	47	48	mA	x8/x16
I_{DD7}	tbd	tbd	mA	x8
	280	289	mA	x16
I_{DD8}	tbd	Tbd	mA	x8
	22	23	mA	x16

Note:

1. Applicable for MR2 setting A6 = 0b and A7 = 0b. Temperature range for IDD6 is 0 – 85°C at commercial temperature, -40 – 85°C at industrial temperature.
2. Applicable for MR2 setting A6 = 0b and A7 = 1b. Temperature range for IDD6ET is 0 – 95°C at commercial temperature & industrial temperature.
3. Some data retains the possibility of future updates.

9 Input/Output Capacitance

9.1 Input/Output Capacitance

Table 44 - DDR3L/DDR3-800/1066/1333/1600 Input/Output Capacitance

Symbol	Parameter		800		1066		1333		1600		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM, DQS, DQS#)	DDR3 (1.5V)	1.4	3.0	1.4	2.7	1.4	2.5	1.4	2.3	pF	1,2,3
		DDR3L (1.35V)	1.4	2.5	1.4	2.5	1.4	2.3	1.4	2.2		
C_{CK}	Input capacitance, CK and CK#		0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2,3
C_{DCK}	Input capacitance delta, CK and CK#		0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
C_{DDQS}	Input/output capacitance delta DQS and DQS#		0	0.2	0	0.2	0	0.15	0	0.15	pF	2,3,5
C_I	Input capacitance (CTRL, ADD, CMD input-only pins)	DDR3 (1.5V)	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	pF	2,3,6
		DDR3L (1.35V)	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2		
C_{DI_CTRL}	Input capacitance delta (All CTRL input-only pins)		-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/CMD input-only pins)		-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
C_{DIO}	Input/output capacitance delta, DQ, DM, DQS, DQS#		-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
C_{ZQ}	Input/output capacitance of ZQ pin		-	3	-	3	-	3	-	3	pF	2,3,12

Note:

1. The DM pin load matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (“Procedure for measuring input capacitance using a vec-tor network analyzer (VNA)”) with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). $V_{DD} = V_{DDQ} =$ 1.35V, $V_{BIAS} = V_{DD}/2$ and on-die termination off.
3. This parameter applies to monolithic devices only, stacked/dual-die devices are not covered here.
4. Absolute value of $C_{CK} – C_{CK\#}$.
5. Absolute value of $C_{IO(DQS)} – C_{IO(DQS\#)}$.
6. C_I applies to ODT, CS#, CKE, A0 – A15, BA0 – BA2, RAS#, CAS#, WE#.
7. C_{DI_CTRL} applies to ODT, CS# and CKE.
8. $C_{DI\_CTRL} = C_{I(CTRL)} – 0.5 \times (C_{I(CLK)} + C_{I(CLK\#)})$.
9. $C_{DI\_ADD\_CMD}$ applies to A0 – A15, BA0 – BA2, RAS#, CAS# and WE#.
10. $C_{DI\_ADD\_CMD} = C_{I(ADD\_CMD)} – 0.5 \times (C_{I(CLK)} + C_{I(CLK\#)})$.
11. $C_{DIO} = C_{IO(DQ,\ DM)} – 0.5 \times (C_{IO(DQS)} + C_{IO(DQS\#)})$.
12. Maximum external load capacitance on ZQ pin: 5pF.

Table 45 - DDR3L/DDR3-1866/2133 Input/Output Capacitance

Symbol	Parameter		1866		2133		Unit	Note
			Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM, DQS, DQS#)	DDR3 (1.5V)	1.4	2.2	1.4	2.1	pF	1,2,3
		DDR3L (1.35V)	1.4	2.1	1.4	2.1		
C_{CK}	Input capacitance, CK and CK#		0.8	1.3	0.8	1.3	pF	2,3
C_{DCK}	Input capacitance delta, CK and CK#		0	0.15	0	0.15	pF	2,3,4
C_{DDQS}	Input/output capacitance delta DQS and DQS#		0	0.15	0	0.15	pF	2,3,5
C_I	Input capacitance (CTRL, ADD, CMD input-only pins)	DDR3 (1.5V)	0.75	1.2	0.75	1.2	pF	2,3,6
		DDR3L (1.35V)	0.75	1.2	0.75	1.2		
C_{DI_CTRL}	Input capacitance delta (All CTRL input-only pins)		-0.4	0.2	-0.4	0.2	pF	2,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/CMD input-only pins)		-0.4	0.4	-0.4	0.4	pF	2,3,9,10
C_{DIO}	Input/output capacitance delta, DQ, DM, DQS, DQS#		-0.5	0.3	-0.5	0.3	pF	2,3,11
C_{ZQ}	Input/output capacitance of ZQ pin		-	3	-	3	pF	2,3,12

Note:

1. The DM pin loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("Procedure for measuring input capacitance using a vec-tor network analyzer(VNA)") with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). $V_{DD} = V_{DDQ} = 1.35V$, $V_{BIAS} = V_{DD}/2$ and on-die termination off.
3. This parameter applies to monolithic devices only, stacked/dual-die devices are not covered here.
4. Absolute value of $C_{CK} - C_{CK\#}$.
5. Absolute value of $C_{IO(DQS)} - C_{IO(DQS\#)}$.
6. C_I applies to ODT, CS#, CKE, A0 – A15, BA0 – BA2, RAS#, CAS#, WE#.
7. C_{DI_CTRL} applies to ODT, CS# and CKE.
8. $C_{DI\_CTRL} = C_{I(CTRL)} - 0.5 \times (C_{I(CLK)} + C_{I(CLK\#)})$.
9. $C_{DI\_ADD\_CMD}$ applies to A0 – A15, BA0 – BA2, RAS#, CAS# and WE#.
10. $C_{DI\_ADD\_CMD} = C_{I(ADD\_CMD)} - 0.5 \times (C_{I(CLK)} + C_{I(CLK\#)})$.
11. $C_{DIO} = C_{IO(DQ, DM)} - 0.5 \times (C_{IO(DQS)} + C_{IO(DQS\#)})$.
12. Maximum external load capacitance on ZQ pin: 5pF.

10 Electronical Characteristics And Timing

10.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3L SDRAM device.

10.1.1 Definition for $t_{CK(avg)}$

$t_{CK(avg)}$ is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$T_{CK(avg)} = \left(\sum_{j=1}^{N} t_{CKj}\right) / N \quad N=200$$

10.1.2 Definition for $t_{CK(abs)}$

$t_{CK(abs)}$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. $T_{CK(abs)}$ is not subject to production test.

10.1.3 Definition for $t_{CH(avg)}$ and $t_{CL(avg)}$

$t_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$T_{CH(avg)} = \left(\sum_{j=1}^{N} t_{CHj}\right) / (N \times t_{CK(avg)}) \quad N=200$$

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$T_{CL(avg)} = \left(\sum_{j=1}^{N} t_{CLj}\right) / (N \times t_{CK(avg)}) \quad N=200$$

10.1.4 Definition for $t_{JIT(per)}$ and $t_{JIT(per, lck)}$

$t_{JIT(per)}$ is defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.
$t_{JIT(per)}$ = min/max of {$t_{CKi} - t_{CK(avg)}$ where I = 1 to 200}.
$T_{JIT(per)}$ defines the single period jitter when the DLL is already locked.
$T_{JIT(per, lck)}$ uses the same definition for single period jitter, during the DLL locking period only.
$T_{JIT(per)}$ and $t_{JIT(per, lck)}$ are not subject to production test.

10.1.5 Definition for $t_{JIT(cc)}$ and $t_{JIT(cc, lck)}$

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.
$T_{JIT(cc)}$ = max of $|\{t_{CKi+1} - t_{CKi}\}|$.
$T_{JIT(cc)}$ defines the cycle to cycle jitter when the DLL is already locked.
$T_{JIT(cc, lck)}$ uses the same definition for cycle to cycle jitter, during the DLL locking period only.
$T_{JIT(cc)}$ and $t_{JIT(cc, lck)}$ are not subject to production test.

10.1.6 Definition for $t_{ERR(nper)}$

t_{ERR} is defined as the cumulative error across multiple consecutive cycles from $t_{CK(avg)}$. t_{ERR} is not subject to production test.

10.2 Refresh Parameters By Device Density

Table 46 - Refresh Parameters by Device Density

Parameter	Symbol		4Gb	Unit	Note
REF command to ACT or REF command time	t_{RFC}		260	ns	-
Average periodic refresh interval	t_{REFI}	0°C ≤ T_{CASE} ≤ 85°C	7.8	µs	-
		85°C < T_{CASE} ≤ 95°C	3.9	µs	-

10.3 Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include t_{CK}, t_{RCD}, t_{RP}, t_{RAS} and t_{RC} for each corresponding bin.

Table 47 - DDR3L/DDR3-1866 Speed Bins and Operating Conditions

Speed Bin			DDR3L/DDR3-1866		Unit	Note
CL-nRCD-nRP			13-13-13			
Parameter		Symbol	Min	Max		
Internal READ command to first data		t_{AA}	13.91(13.125)	20	ns	-
ACT to internal READ or WRITE delay time		t_{RCD}	13.91(13.125)	-	ns	-
PRE command period		t_{RP}	13.91(13.125)	-	ns	-
ACT to PRE command period		t_{RAS}	34	9 × t_{REFI}	ns	-
ACT to ACT or REF command period		t_{RC}	47.91(47.125)	-	ns	-
CL = 6	CWL = 5	$t_{CK(avg)}$	2.5	3.3	ns	1,2,3,5
	CWL = 6	$t_{CK(avg)}$	Reserved		-	4
	CWL = 7,8,9	$t_{CK(avg)}$	Reserved		-	4
CL = 7	CWL = 5	$t_{CK(avg)}$	Reserved		-	4
	CWL = 6	$t_{CK(avg)}$	1.875	< 2.5	ns	1,2,3,4,5
	CWL = 7,8,9	$t_{CK(avg)}$	Reserved		-	4
CL = 8	CWL = 5	$t_{CK(avg)}$	Reserved		-	4
	CWL = 6	$t_{CK(avg)}$	1.875	< 2.5	ns	1,2,3,5
	CWL = 7	$t_{CK(avg)}$	Reserved		-	4
	CWL = 8,9	$t_{CK(avg)}$	Reserved		-	4
CL = 9	CWL = 5,6	$t_{CK(avg)}$	Reserved		-	4
	CWL = 7	$t_{CK(avg)}$	1.5	< 1.875	ns	1,2,3,4,5
	CWL = 8	$t_{CK(avg)}$	Reserved		-	4
	CWL = 9	$t_{CK(avg)}$	Reserved		-	4
CL = 10	CWL = 5,6	$t_{CK(avg)}$	Reserved		-	4
	CWL = 7	$t_{CK(avg)}$	1.5	< 1.875	ns	1,2,3,5
	CWL = 8	$t_{CK(avg)}$	Reserved		-	4
CL = 11	CWL = 5,6,7	$t_{CK(avg)}$	Reserved		-	4
	CWL = 8	$t_{CK(avg)}$	1.25	< 1.5	ns	1,2,3,4,5
	CWL = 9	$t_{CK(avg)}$	Reserved		-	4
CL = 13	CWL = 5,6,7,8	$t_{CK(avg)}$	Reserved		-	4
	CWL = 9	$t_{CK(avg)}$	1.07	< 1.25	ns	1,2,3
Supported CL Settings			6,7,8,9,10,11,13		nCK	-
Supported CWL Settings			5,6,7,8,9		nCK	-

Table 48 - DDR3L/DDR3-2133 Speed Bins and Operating Conditions

Speed Bin			DDR3L/DDR3-2133		Unit	Note
CL-nRCD-nRP			14-14-14			
Parameter		Symbol	Min	Max		
Internal READ command to first data		t_{AA}	13.09	20	ns	-
ACT to internal READ or WRITE delay time		t_{RCD}	13.09	-	ns	-
PRE command period		t_{RP}	13.09	-	ns	-
ACT to PRE command period		t_{RAS}	33	9 × t_{REFI}	ns	-
ACT to ACT or REF command period		t_{RC}	46.09	-	ns	-
CL = 5	CWL = 5	$t_{CK(avg)}$	Reserved		-	4
	CWL = 6,7,8,9,10	$t_{CK(avg)}$	Reserved		-	4
CL = 6	CWL = 5	$t_{CK(avg)}$	2.5	3.3	ns	1,2,3,6
	CWL = 6	$t_{CK(avg)}$	Reserved		-	4
	CWL = 7,8,9,10	$t_{CK(avg)}$	Reserved		-	4
CL = 7	CWL = 5	$t_{CK(avg)}$	Reserved		-	4
	CWL = 6	$t_{CK(avg)}$	1.875	< 2.5	ns	1,2,3,6
	CWL = 7	$t_{CK(avg)}$	Reserved		-	4
	CWL = 8,9,10	$t_{CK(avg)}$	Reserved		-	4
CL = 8	CWL = 5	$t_{CK(avg)}$	Reserved		-	4
	CWL = 6	$t_{CK(avg)}$	1.875	< 2.5	ns	1,2,3,6
	CWL = 7	$t_{CK(avg)}$	Reserved		-	4
	CWL = 8,9,10	$t_{CK(avg)}$	Reserved		-	4
CL = 9	CWL = 5,6	$t_{CK(avg)}$	Reserved		-	4
	CWL = 7	$t_{CK(avg)}$	1.5	< 1.875	ns	1,2,3,4,6
	CWL = 8	$t_{CK(avg)}$	Reserved		-	4
	CWL = 9,10	$t_{CK(avg)}$	Reserved		-	4
CL = 10	CWL = 5,6	$t_{CK(avg)}$	Reserved		-	4
	CWL = 7	$t_{CK(avg)}$	1.5	< 1.875	ns	1,2,3,6
	CWL = 8	$t_{CK(avg)}$	Reserved		-	4
	CWL = 9	$t_{CK(avg)}$	Reserved		-	4
	CWL = 10	$t_{CK(avg)}$	Reserved		-	4
CL = 11	CWL = 5,6,7	$t_{CK(avg)}$	Reserved		-	4
	CWL = 8	$t_{CK(avg)}$	1.25	< 1.5	ns	1,2,3,6
	CWL = 9	$t_{CK(avg)}$	Reserved		-	4
	CWL = 10	$t_{CK(avg)}$	Reserved		-	4
CL = 13	CWL = 5,6,7,8	$t_{CK(avg)}$	Reserved		-	4
	CWL = 9	$t_{CK(avg)}$	1.07	< 1.25	ns	1,2,3,6
	CWL = 10	$t_{CK(avg)}$	Reserved		-	4
CL = 14	CWL = 5,6,7,8,9	$t_{CK(avg)}$	Reserved		-	4
	CWL = 10	$t_{CK(avg)}$	0.938	< 1.07	ns	1,2,3
Supported CL Settings			5,6,7,8,9,10,11,13,14		nCK	-
Supported CWL Settings			5,6,7,8,9,10		nCK	-

10.3.1 Speed Bin Table Note

Note:

1. The CL setting and CWL setting result in $t_{CK(avg)min}$ and $t_{CK(avg)max}$ requirements. When selecting $t_{CK(avg)}$, both need to be fulfilled requirements from CL setting as well as requirements from CWL setting.
2. $t_{CK(avg)min}$ limits: since CAS Latency is not purely analog-data and strobe output are synchronized by the DLL-all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{CK(avg)}$

value (3.0, 2.5, 1.875, 1.5, 1.25,1.07 or 0.938ns) when calculating CL [nCK] = t_{AA} [ns]/$t_{CK(avg)}$ [ns], rounding up to the next "Supported CL", where $t_{CK(avg)}$ = 3.0ns should only be used for CL = 5 calculation.

3. $t_{CK(avg)max}$ limits: calculate $t_{CK(avg)}$ = t_{Aamax}/CL SELECTED and round the resulting $t_{CK(avg)}$ down to the next valid speed bin (3.3, 2.5, 1.875, 1.5, 1.25, 1.07 or 0.938ns). This result is $t_{CK(avg)max}$ corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR3L/DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/Characterization.
6. Any DDR3L/DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/Characterization.
7. DDR3L-800 AC timing apply if DRAM operates at lower than 800MT/s data rate.
8. For devices supporting optional down binning to CL = 11, CL = 9 and CL = 7, t_{AA}/t_{RCD}/t_{Rpmin} must be 13.125ns. SPD setting must be programed to match.

11 ELECTRICAL CHARACTERISTICS AND AC TIMING

11.1 Timing Parameters for DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600 Speed Bins

Table 49 - Timing Parameters by Speed Bin

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Minimum clock cycle time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	-	8	-	8	-	8	-	ns	6
Average clock period	$t_{CK(avg)}$	See Standard Speed Bins								-	-
Average high pulse width	$t_{CH(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	-
Average low pulse width	$t_{CL(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	-
Absolute clock period	$t_{CK(abs)}$	$t_{CK(avg)min}$ + $t_{JIT(per)min}$	$t_{CK(avg)max}$ + $t_{JIT(per)max}$	$t_{CK(avg)min}$ + $t_{JIT(per)min}$	$t_{CK(avg)max}$ + $t_{JIT(per)max}$	$t_{CK(avg)min}$ + $t_{JIT(per)min}$	$t_{CK(avg)max}$ + $t_{JIT(per)max}$	$t_{CK(avg)min}$ + $t_{JIT(per)min}$	$t_{CK(avg)max}$ + $t_{JIT(per)max}$	ps	-
Absolute clock high pulse width	$t_{CH(abs)}$	0.43	-	0.43	-	0.43	-	0.43	-	$t_{CK(avg)}$	26
Absolute clock low pulse width	$t_{CL(abs)}$	0.43	-	0.43	-	0.43	-	0.43	-	$t_{CK(avg)}$	27
Clock period jitter	$J_{IT(per)}$	-100	100	-90	90	-80	80	-70	70	ps	-
Clock period jitter during DLL locking period	$t_{JIT(per, lck)}$	-90	90	-80	80	-70	70	-60	60	ps	-
Cycle to cycle period jitter	$t_{JIT(cc)}$	200		180		160		140		ps	-
Cycle to cycle period jitter during DLL locking period	$t_{JIT(cc, lck)}$	180		160		140		120		ps	-
Duty cycle jitter	$t_{JIT(duty)}$	-	-	-	-	-	-	-	-	-	-
Cumulative error across 2 cycles	$t_{ERR(2per)}$	-147	147	-132	132	-118	118	-103	103	ps	-
Cumulative error across 3 cycles	$t_{ERR(3per)}$	-175	175	-157	157	-140	140	-122	122	ps	-
Cumulative error across 4 cycles	$t_{ERR(4per)}$	-194	194	-175	175	-155	155	-136	136	ps	-
Cumulative error across 5 cycles	$t_{ERR(5per)}$	-209	209	-188	188	-168	168	-147	147	ps	-
Cumulative error across 6 cycles	$t_{ERR(6per)}$	-222	222	-200	200	-177	177	-155	155	ps	-
Cumulative error across 7 cycles	$t_{ERR(7per)}$	-232	232	-209	209	-186	186	-163	163	ps	-
Cumulative error across 8 cycles	$t_{ERR(8per)}$	-241	241	-217	217	-193	193	-169	169	ps	-
Cumulative error across 9 cycles	$t_{ERR(9per)}$	-249	249	-224	224	-200	200	-175	175	ps	-
Cumulative error across 10 cycles	$t_{ERR(10per)}$	-257	257	-231	231	-205	205	-180	180	ps	-

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across 11 cycles	$t_{ERR(11per)}$	263	263	-237	237	-210	210	-184	184	ps	-
Cumulative error across 12 cycles	$t_{ERR(12per)}$	-269	269	-242	242	-215	215	-188	188	ps	-
Cumulative error across n = 13, 14 . . . 49, 50 cycles	$t_{ERR(nper)}$	$t_{ERR(nper)min} = ((1 + 0.68ln(n)) \times t_{JIT(per)\_total\ min})$								ps	25
		$t_{ERR(nper)max} = ((1 + 0.68ln(n)) \times t_{JIT(per)\_total\ max})$									
Data Timing											
DQS,DQS# to DQ skew, per group, per acces	t_{DQSQ}	-	200	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	t_{QH}	0.38	-	0.38	-	0.38	-	0.38	-	$t_{CK(avg)}$	13, g
DQ low impedance time from CK, CK#	$t_{LZ(DQ)}$	-800	400	-600	300	-500	250	-450	225	ps	13,15,f
DQ high impedance time from CK, CK#	$t_{HZ(DQ)}$	-	400	-	300	-	250	-	225	ps	13,15,f
Data setup time to DQS, DQS# referenced to $V_{IH(AC)}/V_{IL(AC)}$ levels	1.5V										
	$t_{DS(base, AC175)}$	75	-	25	-	-	-	-	-	ps	d,18
	$t_{DS(base, AC150)}$	125	-	75	-	30	-	10	-	ps	d,18
	1.35V										
	$t_{DS(base, AC160)}$	90	-	40	-	-	-	-	-	ps	d,18
	$t_{DS(base, AC135)}$	140	-	90	-	45	-	25	-	ps	d,18
Data hold time from DQS, DQS# referenced to $V_{IH(DC)}/V_{IL(DC)}$ levels	1.5V										
	$t_{DH(base, DC100)}$	150	-	100	-	65	-	45	-	ps	d,18
	1.35V										
	$t_{DH(base, DC90)}$	160	-	110	-	75	-	55	-	ps	d,18
DQ and DM Input pulse width for each input	t_{DIPW}	600	-	490	-	400	-	360	-	ps	29
Data Strobe Timing											
DQS, DQS# differential READ preamble	t_{RPRE}	0.9	Note19	0.9	Note19	0.9	Note19	0.9	Note 19	$t_{CK(avg)}$	13,20,g
DQS, DQS# differential READ preamble	t_{RPST}	0.3	Note11	0.3	Note11	0.3	Note11	0.3	Note 11	$t_{CK(avg)}$	11,13,g
DQS, DQS# differential output high time	t_{QSH}	0.38	-	0.38	-	0.40	-	0.40	-	$t_{CK(avg)}$	13,g
DQS, DQS# differential output low time	t_{QSL}	0.38	-	0.38	-	0.40	-	0.40	-	$t_{CK(avg)}$	13,g
DQS, DQS# differential WRITE preamble	t_{WPRE}	0.9	-	0.9	-	0.9	-	0.9	-	$t_{CK(avg)}$	1
DQS, DQS# differential WRITE preamble	t_{WPST}	0.3	-	0.3	-	0.3	-	0.3	-	$t_{CK(avg)}$	1

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DQS, DQS# rising edge output access time from rising CK, CK#	t_{DQSCK}	-400	400	-300	300	-255	255	-225	225	ps	13,f
DQS and DQS# low-impedance time (Referenced from RL – 1)	$t_{LZ(DQS)}$	-800	400	-600	300	-500	250	-450	225	ps	13,15,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	$t_{HZ(DQS)}$	-	400	-	300	-	250	-	225	ps	13,15,f
DQS and DQS# differential input low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK(avg)}$	30,32
DQS and DQS# differential input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK(avg)}$	31,32
DQS, DQS# rising edge to CK, CK# rising edge	t_{DQSS}	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.27	0.27	$t_{CK(avg)}$	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	t_{DSS}	0.2	-	0.2	-	0.2	-	0.18	-	$t_{CK(avg)}$	c,33
DQS, DQS# falling edge hold time from CK, CK# rising edge	t_{DSH}	0.2	-	0.2	-	0.2	-	0.18	-	$t_{CK(avg)}$	c,33
Command and Address Timing											
DLL locking time	t_{DLLK}	512	-	512	-	512	-	512	-	nCK	-
Internal READ command to PRECHARGE command delay	t_{RTP}	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	nCK	e
Delay from start of internal write transaction to internal READ command	t_{WTR}	Max (4nCK, 7.5ns)	-	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	nCK	e,19
WRITE recovery time	t_{WR}	15	-	15	-	15	-	15	-	ns	e,19
Mode register set command cycle time	t_{MRD}	4	-	4	-	4	-	4	-	nCK	-
Mode register set command update delay	t_{MOD}	Max (12nCK,15ns)	-	Max (12nCK,15ns)	-	Max (12nCK,15ns)	-	Max (12nCK,15ns)	-	nCK	-
ACT to internal READ or WRITE delay time	t_{RCD}	See Standard Speed Bins								-	e
PRE command period	t_{RP}	See Standard Speed Bins								-	e
ACT to ACT or REF command period	t_{RC}	See Standard Speed Bins								-	e
CAS# to CAS# command delay	t_{CCD}	4	-	4	-	4	-	4	-	nCK	-

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Auto-Precharge write recovery precharge time	t_{DALmin}	WR + round up ($t_{RP}/t_{CK(avg)}$)								nCK	-
Multi-Purpose register recovery Time	t_{MPRR}	1	-	1	-	1	-	1	-	nCK	23
ACTIVE to PRECHARGE command period	t_{RAS}	See Standard Speed Bins								-	e
ACTIVE to ACTIVE command period for 1KB page size	t_{RRD}	Max (4nCK,10ns)	-	Max (4nCK,7.5ns)	-	Max (4nCK,6ns)	-	Max (4nCK,6ns)	-	nCK	e
ACTIVE to ACTIVE command period for 2KB page size	t_{RRD}	Max (4nCK,10ns)	-	Max (4nCK,10ns)	-	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	nCK	e
Four activate window for 1KB page size	t_{FAW}	40	-	37.5	-	30	-	30	-	ns	e
Four activate window for 2KB page size	t_{FAW}	50	-	50	-	45	-	40	-	ns	e
Command and address setup time to CK, CK# referenced to $V_{IH(AC)}/V_{IL(AC)}$ levels	1.5V										
	$t_{IS(base, AC175)}$	200	-	125	-	65	-	45	-	ps	b,17
	$t_{IS(base, AC150)}$	350	-	275	-	190	-	170	-	ps	b,17
	1.35V										
	$t_{IS(base, AC160)}$	215	-	140	-	80	-	60	-	ps	b,17
	$t_{IS(base, AC135)}$	365	-	290	-	205	-	185	-	ps	b,17
Command and Address hold time from CK, CK# referenced to $V_{IH(DC)}/V_{IL(DC)}$ levels	1.5V										
	$t_{IH(base, DC100)}$	275	-	200	-	140	-	120	-	ps	b,17
	1.35V										
	$t_{IH(base, DC90)}$	285	-	210	-	150	-	130	-	ps	b,17
Control and Address input pulse width for each input	t_{IPW}	900	-	780	-	620	-	560	-	ps	29
Calibration Timing											

eed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Power-up and RESET calibration time	t_{Zqinit}	Max (512nCK,640 ns)	-	Max (512nCK,640 ns)	-	Max (512nCK,640 ns)	-	Max (512nCK,640 ns)	-	nCK	-
Normal operation full calibration time	t_{Zqoper}	Max (256nCK,320 ns)	-	Max (256nCK, 320 ns)	-	Max (256nCK,320 ns)	-	Max (256nCK,320 ns)	-	nCK	-
Normal operation short calibration short calibration time	t_{ZQCS}	Max (64nCK,80ns)	-	Max (64nCK,80ns)	-	Max (64nCK,80ns)	-	Max (64nCK,80ns)	-	nCK	24
Reset Timing											
Exit Reset from CKE HIGH to a valid command	t_{XPR}	Max (5nCK,t_{RFCmin} + 10ns)	-	Max (5nCK,t_{RFCmin}+ 10ns)	-	Max (5nCK,t_{RFCmin}+ 10ns)	-	Max (5nCK,t_{RFCmin} + 10ns)	-	nCK	-
Self Refresh Timing											
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	Max (5nCK,t_{RFCmin} + 10ns)	-	Max (5nCK,t_{RFCmin}+ 10ns)	-	Max (5nCK,t_{RFCmin}+ 10ns)	-	Max (5nCK,t_{RFCmin} + 10ns)	-	nCK	-
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	$t_{DLLKmin}$	-	$t_{DLLKmin}$	-	$t_{DLLKmin}$	-	$t_{DLLKmin}$	-	nCK	-
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	t_{CKEmin} + 1nCK	-	t_{CKEmin} + 1nCK	-	t_{CKEmin} + 1nCK	-	t_{CKEmin} + 1nCK	-	nCK	-
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max (5nCK,10ns)	-	Max (5nCK,10ns)	-	Max (5nCK,10ns)	-	Max (5nCK,10ns)	-	nCK	-
Valid Clock Requirement before Self Refresh Exit (SRX) or Power Down Exit (PDX) or Reset Exit	t_{CKSRX}	Max (5nCK,10ns)	-	Max (5nCK,10ns)	-	Max (5nCK,10ns)	-	Max (5nCK,10ns)	-	nCK	-
Power Down Timing											
Exit Power Down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	Max (3nCK,7.5ns)	-	Max (3nCK,7.5ns)	-	Max (3nCK,6ns)	-	Max (3nCK,6ns)	-	nCK	-
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	Max (10nCK,24ns)	-	Max (10nCK,24ns)	-	Max (10nCK,24ns)	-	Max (10nCK,24ns)	-	nCK	2
CKE minimum pulse width	t_{CKE}	Max (3nCK,7.5ns)	-	Max (3nCK,5.625 ns)	-	Max (3nCK,5.625 ns)	-	Max (3nCK,5ns)	-	nCK	-

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Command pass disable delay	t_{CPDED}	1	-	1	-	1	-	1	-	nCK	-
Power Down Entry to Exit Timing	t_{PD}	t_{CKEmin}	9 × t_{REFI}	t_{CKEmin}	9 × t_{REFI}	t_{CKEmin}	9 × t_{REFI}	t_{CKEmin}	9 × t_{REFI}	nCK	16
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	1	-	1	-	1	-	nCK	21
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	1	-	1	-	1	-	1	-	nCK	21
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	-
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4 + (t_{WR}/$t_{CK(avg)}$)	-	WL + 4 + (t_{WR}/$t_{CK(avg)}$)	-	WL + 4 + (t_{WR}/$t_{CK(avg)}$)	-	WL + 4 + (t_{WR}/$t_{CK(avg)}$)	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	t_{WRPDEN}	WL + 2 + (t_{WR}/$t_{CK(avg)}$)	-	WL + 2 + (t_{WR}/$t_{CK(avg)}$)	-	WL + 2 + (t_{WR}/$t_{CK(avg)}$)	-	WL + 2 + (t_{WR}/$t_{CK(avg)}$)	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPDEN}$	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	nCK	10
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	1	-	2	-	2	-	nCK	21,22
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MODmin}	-	t_{MODmin}	-	t_{MODmin}	-	t_{MODmin}	-	nCK	-
ODT Timing											
ODT turn on Latency	ODTLon	WL – 2 = CWL + AL – 2								nCK	-
ODT turn off Latency	ODTLoff	WL – 2 = CWL + AL – 2								nCK	-
ODT high time without WRITE command or with WRITE command and BC4	ODTH4	4	-	4	-	4	-	4	-	nCK	-
ODT high time with WRITE command and BL8	ODTH8	6	-	6	-	6	-	6	-	nCK	-
Asynchronous R_{TT} turn-on delay (Power-Down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	2	8.5	2	8.5	ns	-

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Asynchronous R_{TT} turn-off delay (Power-Down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	2	8.5	2	8.5	ns	-
R_{TT} turn-on	t_{AON}	-400	400	-300	300	-250	250	-225	225	ps	7, f
$R_{TT,Nom}$ and $R_{TT(WR)}$ turn-off time from ODTL off reference	t_{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	8,f
R_{TT} dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	f
Write Leveling Timing											
First DQS/DQS# rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	25	-	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS/DQS# crossing	t_{WLS}	325	-	245	-	195	-	165	-	ps	-
Write leveling hold time from rising DQS/DQS# crossing to rising CK, CK# crossing	t_{WLH}	325	-	245	-	195	-	165	-	ps	-
Write leveling output delay	t_{WLO}	0	9	0	9	0	9	0	7.5	ns	-
Write leveling output error	t_{WLOE}	0	2	0	2	0	2	0	2	ns	-

11.2 Timing Parameters for DDR3L-1866 and DDR3L-2133 Speed Bins

Table 50 - Timing Parameters by Speed Bin

Speed		DDR3L/DDR3-1866		DDR3L/DDR3-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Clock Timing							
Minimum clock cycle time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	-	8	-	ns	6
Average clock period	$t_{CK(avg)}$	See Standard Speed Bins				-	-
Average high pulse width	$t_{CH(avg)}$	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	-
Average low pulse width	$t_{CL(avg)}$	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	-
Absolute clock period	$t_{CK(abs)}$	$t_{CK(avg)min}$ + $t_{JIT(per)min}$	$t_{CK(avg)max}$ + $t_{JIT(per)max}$	$t_{CK(avg)min}$ + $t_{JIT(per)min}$	$t_{CK(avg)max}$ + $t_{JIT(per)max}$	ps	-
Absolute clock HIGH pulse width	$t_{CH(abs)}$	0.43	-	0.43	-	$t_{CK(avg)}$	26
Absolute clock LOW pulse width	$t_{CL(abs)}$	0.43	-	0.43	-	$t_{CK(avg)}$	27
Clock period jitter	$t_{JIT(per)}$	-60	60	-50	50	ps	-
Clock period jitter during DLL locking period	$t_{JIT(per,\ lck)}$	-50	50	-40	40	ps	-
Cycle to cycle period jitter	$t_{JIT(cc)}$	120		100		ps	-
Cycle to cycle period jitter during DLL locking period	$t_{JIT(cc,\ lck)}$	100		80		ps	-
Duty cycle jitter	$t_{JIT(duty)}$	-	-	-	-	-	-
Cumulative error across 2 cycles	$t_{ERR(2per)}$	-88	88	-74	74	ps	-
Cumulative error across 3 cycles	$t_{ERR(3per)}$	-105	105	-87	87	ps	-
Cumulative error across 4 cycles	$t_{ERR(4per)}$	-117	117	-97	97	ps	-
Cumulative error across 5 cycles	$t_{ERR(5per)}$	-126	126	-105	105	ps	-
Cumulative error across 6 cycles	$t_{ERR(6per)}$	-133	133	-111	111	ps	-
Cumulative error across 7 cycles	$t_{ERR(7per)}$	-139	139	-116	116	ps	-
Cumulative error across 8 cycles	$t_{ERR(8per)}$	-145	145	-121	121	ps	-
Cumulative error across 9 cycles	$t_{ERR(9per)}$	-150	150	-125	125	ps	-
Cumulative error across 10 cycles	$t_{ERR(10per)}$	-154	154	-128	128	ps	-
Cumulative error across 11 cycles	$t_{ERR(11per)}$	-158	158	-132	132	ps	-
Cumulative error across 12 cycles	$t_{ERR(12per)}$	-161	161	-134	134	ps	-
Cumulative error across n = 13, 14 . . . 49, 50 cycles	$t_{ERR(nper)}$	$t_{ERR(nper)min}$ = ((1 + 0.68ln(n)) × $t_{JIT(per)\_total\ min}$) $t_{ERR(nper)max}$ = ((1 + 0.68ln(n)) × $t_{JIT(per)\_total\ max}$)				ps	25
Data Timing							
DQS,DQS# to DQ skew, per group, per acces	t_{DQSQ}	-	85	-	75	ps	13
DQ output hold time from DQS, DQS#	t_{QH}	0.38	-	0.38	-	$t_{CK(avg)}$	13, g
DQ low impedance time from CK, CK#	$t_{LZ\ (DQ)}$	-390	195	-360	180	ps	13,15,f
DQ high impedance time from CK, CK#	$t_{HZ\ (DQ)}$	-	195	-	180	ps	13,15,f
Data setup time to DQS, DQS# referenced to $V_{IH(AC)}/V_{IL(AC)}$ levels	1.5V						
	$t_{DS(base,\ AC150)}$	-	-	-	-	ps	d,18
	$t_{DS(base,\ AC135)}$	68	-	53	-	ps	d,18
	1.35V						
	$t_{DS(base,\ AC135)}$	70	-	-	-	ps	d,18
Data hold time from DQS, DQS# referenced to $V_{IH(AC)}/V_{IL(AC)}$ levels	1.5V						
	$t_{DH(base,\ DC100)}$	70	-	55	-	ps	d,18
	1.35V						
	$t_{DH(base,\ DC90)}$	75	-	-	-	ps	d,18

Speed		DDR3L/DDR3-1866		DDR3L/DDR3-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
DQ and DM Input pulse width for each input	t_{DIPW}	320	-	280	-	ps	29
Data Strobe Timing							
DQS, DQS# differential READ preamble	t_{RPRE}	0.9	Note 19	0.9	Note 19	$t_{CK(avg)}$	13,20,g
DQS, DQS# differential READ preamble	t_{RPST}	0.3	Note 11	0.3	Note 11	$t_{CK(avg)}$	11,13,g
DQS, DQS# differential output high time	t_{QSH}	0.4	-	0.38	-	$t_{CK(avg)}$	13,g
DQS, DQS# differential output low time	t_{QSL}	0.4	-	0.38	-	$t_{CK(avg)}$	13,g
DQS, DQS# differential WRITE preamble	t_{WPRE}	0.9	-	0.9	-	$t_{CK(avg)}$	1
DQS, DQS# differential WRITE preamble	t_{WPST}	0.3	-	0.3	-	$t_{CK(avg)}$	1
DQS, DQS# rising edge output access time from rising CK, CK#	t_{DQSCK}	-195	195	-180	180	ps	13,f
DQS and DQS# low-impedance time (Referenced from RL – 1)	$t_{LZ(DQS)}$	-390	195	-360	180	ps	13,15,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	$t_{HZ(DQS)}$	-	195	-	180	ps	13,15,f
DQS and DQS# differential input low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	$t_{CK(avg)}$	30,32
DQS and DQS# differential input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	$t_{CK(avg)}$	31,32
DQS, DQS# rising edge to CK, CK# rising edge	t_{DQSS}	-0.27	0.27	-0.27	0.27	$t_{CK(avg)}$	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	t_{DSS}	0.18	-	0.18	-	$t_{CK(avg)}$	c,33
DQS, DQS# falling edge hold time from CK, CK# rising edge	t_{DSH}	0.18	-	0.18	-	$t_{CK(avg)}$	c,33
Command and Address Timing							
DLL locking time	t_{DLLK}	512	-	512	-	nCK	-
Internal READ command to PRECHARGE command delay	t_{RTP}	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	nCK	e
Delay from start of internal WRITE transaction to internal READ command	t_{WTR}	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	nCK	e,19
Write recovery time	t_{WR}	15	-	15	-	ns	e,19
MODE REGISTER SET command cycle time	t_{MRD}	4	-	4	-	nCK	-
MODE REGISTER SET command update delay	t_{MOD}	Max (12nCK,15ns)	-	Max (12nCK,15ns)	-	nCK	-
ACT to internal READ or WRITE delay time	t_{RCD}	See Standard Speed Bins				-	e
PRE command period	t_{RP}	See Standard Speed Bins				-	e
ACT to ACT or REF command period	t_{RC}	See Standard Speed Bins				-	e
CAS# to CAS# command delay	t_{CCD}	4	-	4	-	nCK	-
Auto-precharge write recovery precharge time	t_{DALmin}	WR + roundup (t_{RP} / $t_{CK(avg)}$)				nCK	-
Multi-Purpose register recovery time	t_{MPRR}	1	-	1	-	nCK	23
ACTIVE to PRECHARGE command period	t_{RAS}	See Standard Speed Bins				-	e
ACTIVE to ACTIVE command period for 1KB page size	t_{RRD}	Max (4nCK,5.0ns)	-	Max (4nCK,5.0ns)	-	nCK	e
ACTIVE to ACTIVE command period for 2KB page siz	t_{RRD}	Max (4nCK,6.0ns)	-	Max (4nCK,6.0ns)	-	nCK	e
Four activate window for 1KB page size	t_{FAW}	27	-	25	-	ns	e
Four activate window for 2KB page size	t_{FAW}	35	-	35	-	ns	e
Command and address setup time to CK, CK# referenced to $V_{IH(AC)}$/$V_{IL(AC)}$ levels	1.5V						
	$t_{IS(base, AC150)}$	-	-	-	-	ps	b,17
	$t_{IS(base, AC125)}$	150	-	135	-	ps	b,17
	1.35V						

Speed		DDR3L/DDR3-1866		DDR3L/DDR3-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
	$t_{IS(base, AC135)}$	65	-	-	-	ps	b,17
	$t_{IS(base, AC125)}$	150	-	-	-	ps	b,17
Command and Address hold time from CK, CK# referenced to $V_{IH(DC)}/V_{IL(DC)}$ levels	1.5V						
	$t_{IH(base, DC100)}$	100	-	95	-	ps	b,17
	1.35V						
	$t_{IH(base, DC90)}$	110	-	-	-	ps	b,17
Control and address Input pulse width for each input	t_{IPW}	535	-	470	-	ps	29
Calibration Timing							
Power-up and Reset calibration time	t_{Zqinit}	Max (512nCK,640 ns)	-	Max (512nCK,640 ns)	-	nCK	-
Normal operation Full calibration time	t_{Zqoper}	Max (256nCK,320 ns)	-	Max (256nCK,320 ns)	-	nCK	-
Normal operation short calibration short calibration time	t_{ZQCS}	Max (64nCK,80ns)	-	Max (64nCK,80ns)	-	nCK	24
Reset Timing							
Exit Reset from CKE High to a valid command	t_{XPR}	Max (5nCK,t_{RFCmin} + 10ns)	-	Max (5nCK,t_{RFCmin} + 10ns)	-	nCK	-
Self Refresh Timing							
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	Max (5nCK,t_{RFCmin} + 10ns)	-	Max (5nCK,t_{RFCmin} + 10ns)	-	nCK	-
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	$t_{DLLKmin}$	-	$t_{DLLKmin}$	-	nCK	-
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	t_{CKEmin} + 1nCK	-	t_{CKEmin} + 1nCK	-	nCK	-
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max (5nCK,10ns)	-	Max (5nCK,10ns)	-	nCK	-
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	Max (5nCK,10ns)	-	Max (5nCK,10ns)	-	nCK	-
Power Down Timing							
Exit Power Down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	Max (3nCK,6ns)	-	Max (3nCK,6ns)	-	nCK	-
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	Max (10nCK,24ns)	-	Max (10nCK,24ns)	-	nCK	2
CKE minimum pulse width	t_{CKE}	Max (3nCK,5ns)	-	Max (3nCK,5ns)	-	nCK	-
Command pass disable delay	t_{CPDED}	2	-	2	-	nCK	-
Power Down Entry to Exit Timing	t_{PD}	t_{CKEmin}	9 × t_{REFI}	t_{CKEmin}	9 × t_{REFI}	nCK	16
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	2	-	nCK	21

Speed		DDR3L/DDR3-1866		DDR3L/DDR3-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	1	-	2	-	nCK	21
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 + 1	-	RL + 4 + 1	-	nCK	-
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4 + ($t_{WR}/t_{CK(avg)}$)	-	WL + 4 + ($t_{WR}/t_{CK(avg)}$)	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	t_{WRPDEN}	WL + 2 + ($t_{WR}/t_{CK(avg)}$)	-	WL + 2 + ($t_{WR}/t_{CK(avg)}$)	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPDEN}$	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	10
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	2	-	nCK	21,22
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MODmin}	-	t_{MODmin}	-	-	-
ODT Timing							
ODT turn on Latency	ODTLon	WL – 2 = CWL + AL – 2				nCK	-
ODT turn off Latency	ODTLoff	WL – 2 = CWL + AL – 2				nCK	-
ODT high time without WRITE command or with WRITE command and BC4	ODTH4	4	-	4	-	nCK	-
ODT high time with WRITE command and BL8	ODTH8	6	-	6	-	nCK	-
Asynchronous R_{TT} turn-on delay (Power-Down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	ns	-
Asynchronous R_{TT} turn-off delay (Power-Down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	ns	-
R_{TT} turn-on	t_{AON}	-195	195	-180	180	ps	7, f
$R_{TT,Nom}$ and $R_{TT(WR)}$ turn-off time from ODTL off reference	t_{AOF}	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	8,f
R_{TT} dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	f
Write Leveling Timing							
First DQS/DQS# rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS/DQS# crossing	t_{WLS}	140	-	125	-	ps	-
Write leveling hold time from rising DQS/DQS# crossing to rising CK, CK#	t_{WLH}	140	-	125	-	ps	-
Write leveling output delay	t_{WLO}	0	7.5	0	7.5	ns	-
Write leveling output error	t_{WLOE}	0	2	0	2	ns	-

11.3 Jitter Notes

Note:

1. Unit '$t_{CK(avg)}$' represents the actual $t_{CK(avg)}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex tMRD = 4 [nCK] means, if one MODE REGISTER SET command is registered at Tm, another MODE REGISTER SET command may be registered at Tm + 4, even if (Tm + 4 – Tm) is 4 x $t_{CK(avg)}$ + $t_{ERR(4per)min}$.
2. These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.)

transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, $t_{JIT(cc)}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

3. These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)#) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, $t_{JIT(cc)}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
4. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U) #) crossing.
5. For these parameters, the DDR3 SDRAM device supports t_{nPARAM} [nCK] = RU {t_{PARAM} [ns]/$t_{CK(avg)}$ [ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support t_{nRP} = RU {$t_{RP}/t_{CK(avg)}$}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3L/DDR3-800 6-6-6, of which t_{RP} = 15ns, the device will support t_{nRP} = RU {$t_{RP}/t_{CK(avg)}$} = 6, as long as the input clock jitter specifications are met, i.e. PRECHARGE command at Tm and ACTIVE command at Tm+6 is valid even if (Tm + 6 – Tm) is less than 15ns due to input clock jitter.
6. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(mper)}$, act of the input clock, where 2 ≤ m ≤ 12. (output deratings are relative to the SDRAM input clock.)
   For example, if the measured jitter into a DDR3L/DDR3-800 SDRAM has $t_{ERR(mper),act,min}$ = - 172ps and $t_{ERR(mper),act,max}$ = + 193ps, then $t_{DQSCK,min(derated)}$ = $t_{DQSCK,min}$ – $t_{ERR(mper),act,max}$ = - 400ps – 193ps = - 593ps and $t_{DQSCK,max(derated)}$ = $t_{DQSCK,max}$ - $t_{ERR(mper),act,min}$ = 400ps + 172ps = + 572ps. Similarly, $t_{LZ(DQ)}$ for DDR3L-800 derates to $t_{LZ(DQ),min(derated)}$ = - 800ps – 193ps = - 993ps and $t_{LZ(DQ),max(derated)}$ = 400ps + 172ps = + 572ps. (Caution on the min/max usage).
   Note that $t_{ERR(mper),act,min}$ is the minimum measured value of $t_{ERR(nper)}$ where 2 ≤ n ≤ 12, and $t_{ERR(mper),act,max}$ is the maximum measured value of $t_{ERR(nper)}$ where 2 ≤ n ≤12.
7. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per)}$, act of the input clock. (output deratings are relative to the SDRAM input clock) For example, if the measured jitter into a DDR3L/DDR3-800 SDRAM has $t_{CK(avg),act}$ = 2500ps, $t_{JIT(per),act,min}$ = - 72ps and $t_{JIT(per),act,max}$ = + 93ps, then $t_{RPRE,min(derated)}$ = $t_{RPRE,min}$ + $t_{JIT(per),act,min}$ = 0.9 x $t_{CK(avg),act}$ + $t_{JIT(per),act,min}$ = 0.9 x 2500ps – 72ps = + 2178ps. Similarly, $t_{QH,min(derated)}$ = $t_{QH,min}$ + $t_{JIT(per),act,min}$ = 0.38 x $t_{CK(avg),act}$ + $t_{JIT(per),act,min}$ = 0.38 x 2500ps – 72ps = + 878ps. (Caution I min/max usage.)

11.4 Timing Parameter Notes

Note:

1. Actual value dependant upon measurement level definitions. See “Method for calculating t_{WPRE} transitions and endpoints” and “Method for calculating t_{WPST} transitions and endpoints”.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, t_{REFI}.
7. For definition of R_{TT} turn-on time t_{AON}.
8. For definition of R_{TT} turn-off time t_{AOF}.
9. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR}/t_{CK} to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum READ postamble is bound by $t_{DQSCKmin}$ plus t_{QSHmin} on the left side and $t_{HZ(DQS)max}$ on the right side. See “Clock to data strobe relationship”.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
13. Value is only valid for R_{ON34}.
14. Single-ended signal parameter.
15. t_{REFI} depends on T_{OPER}.
16. $t_{IS(base)}$ and $t_{IH(base)}$ values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, $V_{REF(DC)}$ = $V_{REFDQ(DC)}$. For input only pins except RESET#, $V_{REF(DC)}$ = $V_{REFCA(DC)}$. See “Address/ Command Setup, Hold and Derating” in Section 11.5.
17. $t_{DS(base)}$ and $t_{DH(base)}$ values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, $V_{REF(DC)}$ = $V_{REFDQ(DC)}$. For input only pins except RESET#, $V_{REF(DC)}$ = $V_{REFCA(DC)}$. See “Data Setup, Hold and Slew Rate Derating” in Section 11.6.
18. Start of internal write transaction is defined as follows:
    For BL8 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

19. The maximum READ preamble is bound by $t_{LZ(DQS)min}$ on the left side and $t_{DQSCKmax}$ on the right side.
20. CKE is allowed to be registered LOW while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power-down I_{DD} spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once $t_{REFPDENmin}$ is satisfied, there are cases where additional time such as $t_{XPDLLmin}$ is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct aminimum of 0.5% (ZQ Correction) of R_{ON} and R_{TT} impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{V driftrate})}$$

    where Tsens = max ($dR_{TTd}T$, $dR_{ON}dTM$) and Vsens = max ($dR_{TT}dV$, $dR_{ON}dVM$) define the SDRAM temperature and voltage sensitivities.
    For example, if Tsens = 1.5%/℃, Vsens = 0.15%/mV, Tdriftrate = 1℃/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. $t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. $t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The $t_{IS(base, AC150)}$ specifications are adjusted from the $t_{IS(base)}$ specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175 mv – 150mV)/1V/ns].
28. Pulse width of an input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
29. t_{DQSL} describes the instantaneous differential input low pulse width on DQS – DQS#, as measured from one falling edge to the next consecutive rising edge.
30. t_{DQSH} describes the instantaneous differential input high pulse width on DQS – DQS#, as measured from one rising edge to the next consecutive falling edge.
31. $t_{DQSH, act} + t_{DQSL, act} = 1t_{CK, act}$ with $t_{XYZ, act}$ being the actual measured value of the respective timing parameter in the application.
32. $t_{DSH, act} + t_{DSS, act} = 1t_{CK, act}$ with $t_{XYZ, act}$ being the actual measured value of the respective timing parameter in the application.

11.5 Address/Command Setup, Hold and Derating

For all input signals the total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the datasheet $t_{IS(base)}$ and $t_{IH(base)}$ value (see Table 51) to the Δt_{IS} and Δt_{IH} derating value (see Table 53) respectively.

Example: $t_{IS\ (total\ setup\ time)} = t_{IS(base)} + \Delta t_{IS}$.

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(DC)}$ to AC region', use nominal slew rate for derating value (see Figure 25). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(DC)}$ to AC region', the slew rate of a tangent line to the actual signal from the AC level to $V_{REF(DC)}$ level is used for derating value (see Figure 27).

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'DC to $V_{REF(DC)}$ region', use nominal slew rate for derating value (see Figure 26). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for derating value (see Figure 27).

For a valid transition the input signal has to remain above/below $V_{IH/IL(AC)}$ for some time t_{VAC} (see Table 60). Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach $V_{IH/IL(AC)}$. For slew rates in between the values listed in Table 53, the derating values may obtain by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table 51- ADD/CMD Setup and Hold Base-Values for 1V/ns (1.35V)

Symbol	Reference	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	Unit
$t_{IS(base, AC160)}$	$V_{IH/L(AC)}$	215	140	80	60	-	-	ps
$t_{IS(base, AC135)}$	$V_{IH/L(AC)}$	365	290	205	185	65	60	ps
$t_{IS(base, AC125)}$	$V_{IH/L(AC)}$	-	-	-	-	150	135	ps
$t_{IH(base, DC90)}$	$V_{IH/L(DC)}$	285	210	150	130	110	95	ps

Note:

1. AC/DC referenced for 1V/ns Address/Command slew rate and 2V/ns differential CK-CK# slew rate.
2. The $t_{IS(base, AC135)}$ specifications are adjusted from the $t_{IS(base, AC160)}$ specification by adding an additional 125ps for DDR3L- 800/1066 or 100ps for DDR3L-1333/1600 of derating to accommodate for the lower alternate threshold of 135mV and another 25ps to account for the earlier reference point [(160mV – 135mV)/1V/ns].
3. The $t_{IS(base, AC125)}$ specifications are adjusted from the $t_{IS(base, AC135)}$ specification by adding an additional 75ps for DDR3L-1866 and 65ps for DDR3L-2133 to accommodate for the lower alternate threshold of 125mV and another 10ps to account for the earlier reference point [(135mV – 125mV)/1V/ns].

Table 52 - ADD/CMD Setup and Hold Base-Values for 1V/ns (1.5V)

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Unit
$t_{IS(base, AC175)}$	$V_{IH/L(AC)}$	200	125	65	45	-	-	ps
$t_{IS(base, AC150)}$	$V_{IH/L(AC)}$	350	275	190	170	-	-	ps
$t_{IS(base, AC135)}$	$V_{IH/L(AC)}$	-	-	-	-	65	60	ps
$t_{IS(base, AC125)}$	$V_{IH/L(AC)}$	-	-	-	-	150	135	ps
$t_{IH(base, DC90)}$	$V_{IH/L(DC)}$	275	200	140	120	100	95	ps

Note:

1. AC/DC referenced for 1V/ns Address/Command slew rate and 2V/ns differential CK – CK# slew rate.

Table 53 - Derating value DDR3L-800/1066/1333/1600 t_{IS}/t_{IH} – AC/DC based AC160 Threshold (1.35V)

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC based AC160 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 160mV$, $V_{IL(AC)} = V_{REF(DC)} - 160mV$																	
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate V/ns	2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
	1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-1	-3	-1	-3	-1	-3	7	5	15	13	23	21	31	31	39	47
	0.8	-3	-8	-3	-8	-3	-8	5	1	13	9	21	17	29	27	37	43
	0.7	-5	-13	-5	-13	-5	-13	3	-5	11	3	19	11	27	21	35	37
	0.6	-8	-20	-8	-20	-8	-20	0	-12	8	-4	16	4	24	14	32	30
	0.5	-20	-30	-20	-30	-20	-30	-12	-22	-4	-14	4	-6	12	4	20	20
	0.4	-40	-45	-40	-45	-40	-45	-32	-37	-24	-29	-16	-21	-8	-11	0	5

Table 54 - Derating value DDR3L-800/1066/1333/1600 t_{IS}/t_{IH} – AC/DC based Alternate AC135 Threshold (1.35V)

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC based Alternate AC135 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 135mV$, $V_{IL(AC)} = V_{REF(DC)} - 135mV$																	
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate V/ns	2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
	1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-3	2	-3	2	-3	10	5	18	13	26	21	34	31	42	47
	0.8	3	-8	3	-8	3	-8	11	1	19	9	27	17	35	27	43	43
	0.7	6	-13	6	-13	6	-13	14	-5	22	3	30	11	38	21	46	37
	0.6	9	-20	9	-20	9	-20	17	-12	25	-4	33	4	41	14	49	30
	0.5	5	-30	5	-30	5	-30	13	-22	21	-14	29	-6	37	4	45	20
	0.4	-3	-45	-3	-45	-3	-45	6	-37	14	-29	22	-21	30	-11	38	5

Table 55 - Derating value DDR3L-1866/2133 t_{IS}/t_{IH} – AC/DC based Alternate AC125 Threshold (1.35V)

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC based Alternate AC125 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 125mV$, $V_{IL(AC)} = V_{REF(DC)} - 125mV$																	
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate V/ns	2.0	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
	1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	35	31	43	47
	0.8	6	-8	6	-8	6	-8	14	1	22	9	30	17	38	27	46	43
	0.7	10	-13	10	-13	10	-13	18	-5	26	3	34	11	42	21	50	37
	0.6	16	-20	16	-20	16	-20	24	-12	32	4	40	-4	48	14	56	30
	0.5	15	-30	15	-30	15	-30	23	-22	31	-14	39	-6	47	4	55	20
	0.4	13	-45	13	-45	13	-45	21	-37	29	-29	37	-21	45	-11	53	5

Table 56 - Derating value DDR3-800/1066/1333/1600 t_{IS}/t_{IH} – AC/DC based AC175 Threshold (1.5V)

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC based AC175 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 175mV$, $V_{IL(AC)} = V_{REF(DC)} - 175mV$																	
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Table 57 - Derating value DDR3-800/1066/1333/1600 t_{IS}/t_{IH} – AC/DC based AC150 Threshold (1.5V)

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC based Alternate AC150 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 150mV$, $V_{IL(AC)} = V_{REF(DC)} - 150mV$																	
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Table 58 - Derating value DDR3-1866/2133 t_{IS}/t_{IH} – AC/DC based AC135 Threshold (1.5V)

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC based Alternate AC135 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 135mV$, $V_{IL(AC)} = V_{REF(DC)} - 135mV$																	
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate V/ns	2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

Table 59 - Derating value DDR3-1866/2133 t_{IS}/t_{IH} – AC/DC based AC125 Threshold (1.5V)

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC based Alternate AC125 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 125mV$, $V_{IL(AC)} = V_{REF(DC)} - 125mV$																	
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtI_S	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate V/ns	2.0	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
	1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
	0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
	0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
	0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
	0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
	0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

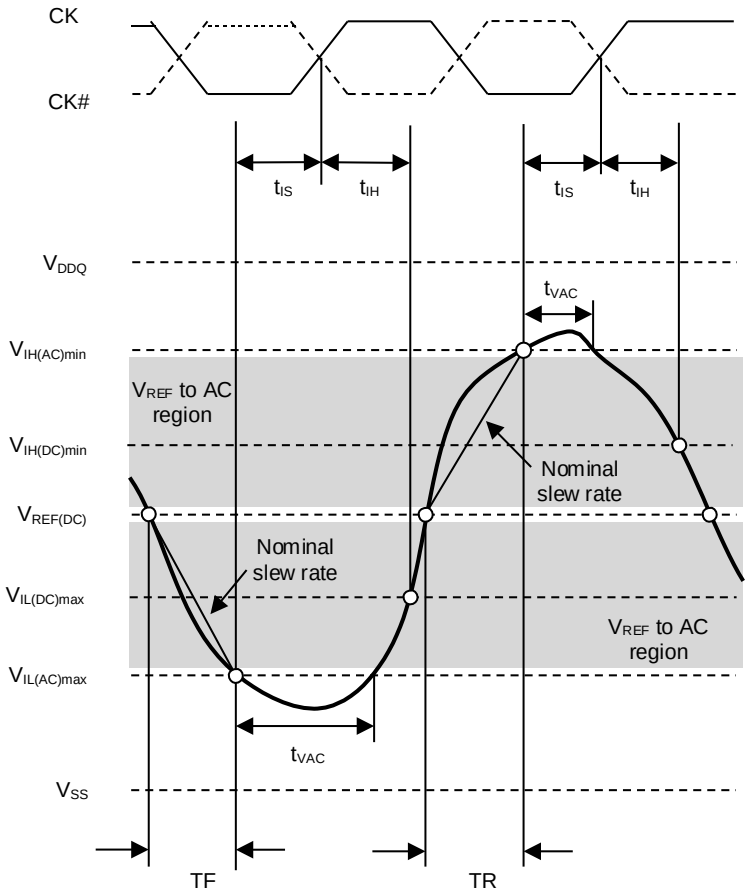
Table 60 - Required minimum time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid ADD/CMD transition (1.35V)

Slew Rate [V/ns]	DDR3				DDR3L			
	800/1066/1333/1600		1866/2133		800/1066/1333/1600		1866/2133	
	175mV [ps]	150mV [ps]	135mV [ps]	125mV [ps]	160mV [ps]	135mV [ps]	135mV [ps]	125mV [ps]
>2.0	75	175	168	173	200	213	200	205
2.0	57	170	168	173	200	213	200	205
1.5	50	167	145	152	173	190	178	184
1.0	38	130	100	110	120	145	133	143
0.9	34	113	85	96	102	130	118	129
0.8	29	93	66	79	80	111	99	111
0.7	22	66	42	56	51	87	75	89
0.6	Note	30	10	27	13	55	43	59
0.5	Note	Note	Note	Note	Note	10	Note	18
<0.5	Note	Note	Note	Note	Note	10	Note	18

Note:

1. Rising input signal shall become equal to or greater than $V_{IL(AC)}$ level and falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

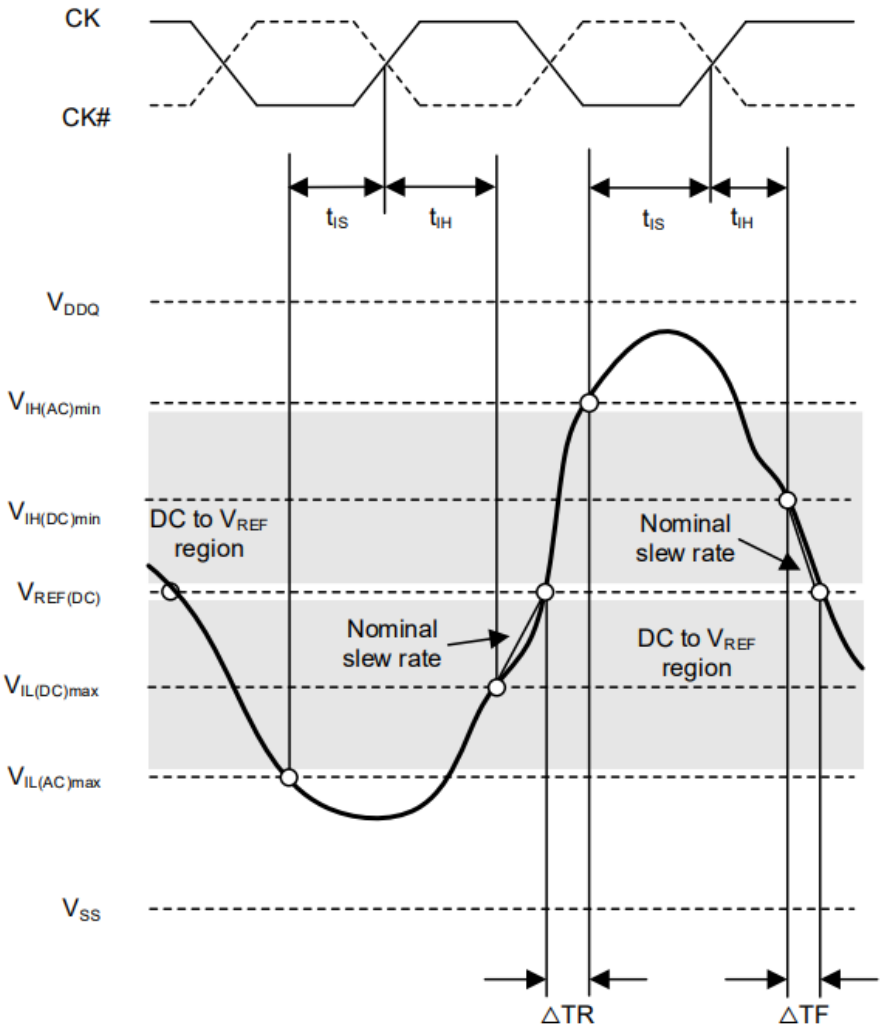
Figure 25 - Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} (for ADD/CMD with respect to clock)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)min} - V_{REF(dc)}}{\Delta TR}$$

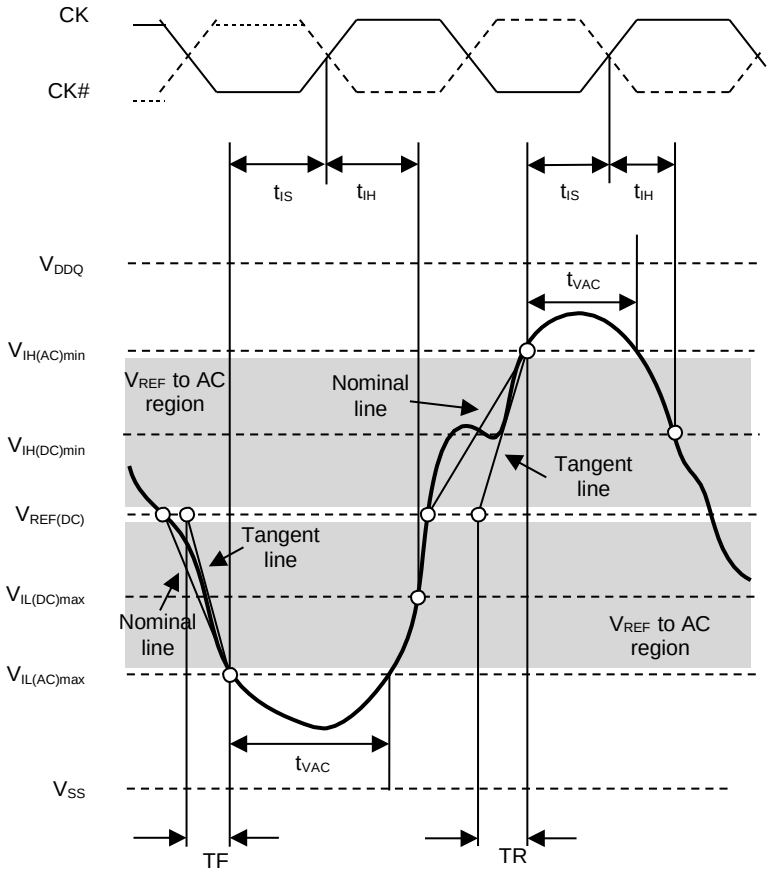
Figure 26 - Illustration of nominal slew rate for hold time t_{IH} (for ADD/CMD with respect to clock)



$$\text{Hold Slew Rate Rising Signal} = \frac{[V_{REF(dc)} - V_{IL(dc)max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{[V_{IH(dc)min} - V_{REF(dc)}]}{\Delta TF}$$

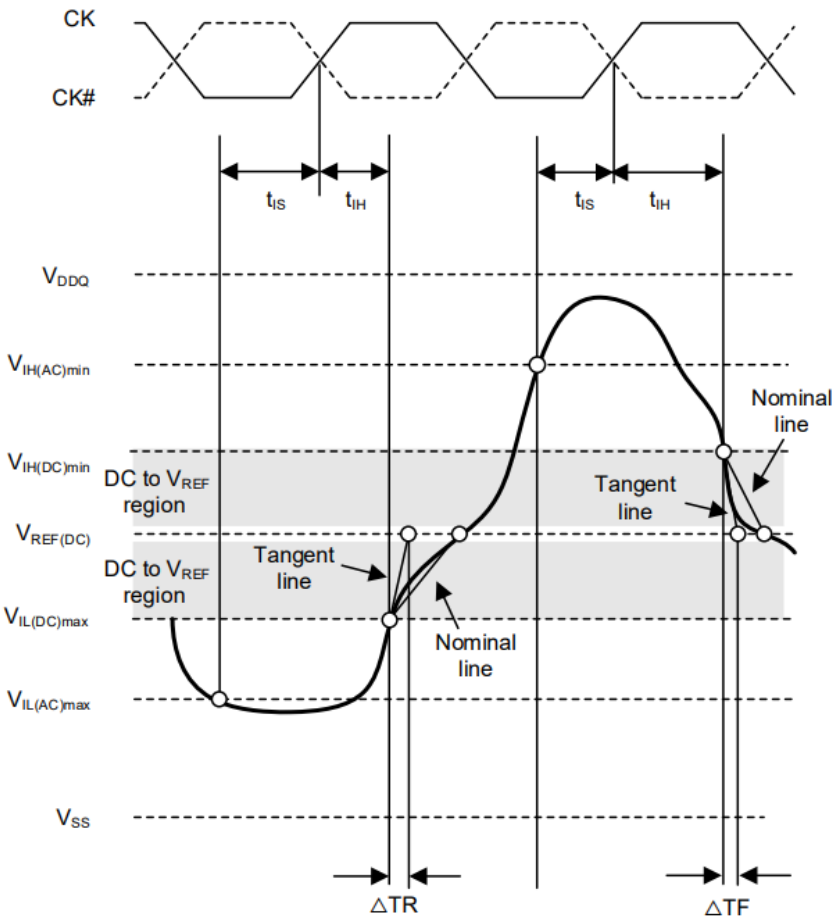
Figure 27 - Illustration of tangent line for setup time t_{IS} (for ADD/CMD with respect to clock)



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{Targent line } [V_{IH(ac)min} - V_{REF(dc)}]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{Targent line } [V_{REF(dc)} - V_{IL(ac)max}]}{\Delta TF}$$

Figure 28 - Illustration of tangent line for hold time t_{IH} (for ADD/CMD with respect to clock)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{REF(dc)} - V_{IL(dc)max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{IH(dc)min} - V_{REF(dc)}]}{\Delta TF}$$

11.6 Data Setup, Hold and Slew Rate Derating

For all input signals the total $t_{DS\ (setup\ time)}$ and $t_{DH\ (hold\ time)}$ required is calculated by adding the data sheet $t_{DS(base)}$ and $t_{DH(base)}$ valuesto the Δt_{DS} and Δt_{DH} derating value respectively.

Example: $t_{DS\ (total\ setup\ time)} = t_{DS(base)} + \Delta t_{DS}$.

Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$ (see Figure 29). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(DC)}$ to AC region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(DC)}$ to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 31).

Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$ (see Figure 30). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to $V_{REF(DC)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rateline anywhere between shaded 'DC to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for derating value (see Figure 32).

For a valid transition the input signal has to remain above/below $V_{IH/IL(AC)}$ for some time t_{VAC}. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(AC)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(AC)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table 61 - Data Setup and Hold Base-Values (1.35V)

Symbol	Reference	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	Unit	Note
$t_{DS(base, AC160)}$	$V_{IH/L(AC)}$ SR = 1V/ns	90	40	-	-	-	-	ps	2
$t_{DS(base, AC135)}$	$V_{IH/L(AC)}$ SR = 1V/ns	140	90	45	25	-	-	ps	2
$t_{DS(base, AC130)}$	$V_{IH/L(AC)}$ SR = 2V/ns	-	-	-	-	70	55	ps	1
$t_{DH(base, DC90)}$	$V_{IH/L(DC)}$ SR = 2V/ns	-	-	-	-	75	60	ps	2
$t_{DH(base, DC90)}$	$V_{IH/L(DC)}$ SR = 1V/ns	160	110	75	55	-	-	ps	1

Table 62 - Data Setup and Hold Base-Values (1.5V)

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Unit	Note
$t_{DS(base, AC175)}$	$V_{IH/L(AC)}$ SR = 1V/ns	75	25	-	-	-	-	ps	2
$t_{DS(base, AC150)}$	$V_{IH/L(AC)}$ SR = 1V/ns	125	75	30	10	-	-	ps	2
$t_{DS(base, AC135)}$	$V_{IH/L(AC)}$ SR = 1V/ns	165	115	60	40	-	-	ps	2,3
$t_{DS(base, AC135)}$	$V_{IH/L(AC)}$ SR = 2V/ns	-	-	-	-	68	53	ps	1
$t_{DH(base, DC100)}$	$V_{IH/L(DC)}$ SR = 1V/ns	150	100	65	45	-	-	ps	3
$t_{DH(base, DC100)}$	$V_{IH/L(DC)}$ SR = 2V/ns	-	-	-	-	70	55	ps	1

Note:

1. AC/DC referenced for 2V/ns DQ-slew rate and 4V/ns DQS slew rate.
2. AC/DC referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate. Optional in DDR3L SDRAM.

Table 63 - Derating values for DDR3L-800/1066 t_{DS}/t_{DH} – (AC160) (1.35V)

AC160 Threshold-> $V_{IH(AC)} = V_{REF(DC)} + 160mV$, $V_{IL(AC)} = V_{REF(DC)} - 160mV$																	
DDR3L		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ Slew Rate V/ns	2.0	80	45	80	45	80	45	-	-	-	-	-	-	-	-	-	-
	1.5	53	30	53	30	53	30	61	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-1	-3	-1	-3	7	5	15	13	23	21	-	-	-	-
	0.8	-	-	-	-	-3	-8	5	1	13	9	21	17	29	27	-	-
	0.7	-	-	-	-	-	-	3	-5	11	3	19	11	27	21	35	37
	0.6	-	-	-	-	-	-	-	-	8	-4	16	4	24	14	32	30
	0.5	-	-	-	-	-	-	-	-	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-8	-11	0	5

Note:

1. Cell contents which is '-' are defined as 'not supported'.

Table 64 - Derating values for DDR3L-800/1066/1333/1600 t_{DS}/t_{DH} – (AC135) (1.35V)

AC135 Threshold-> $V_{IH(AC)} = V_{REF(DC)} + 135mV$, $V_{IL(AC)} = V_{REF(DC)} - 135mV$																	
DDR3L		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ Slew Rate V/ns	2.0	68	45	68	45	68	45	-	-	-	-	-	-	-	-	-	-
	1.5	45	30	45	30	45	34	53	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
	0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
	0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
	0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	30
	0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

Note:

1. Cell contents which is '-' are defined as 'not supported'.

Table 65 - Derating values for DDR3L-1866 t_{DS}/t_{DH} – (AC130) (1.35V)

AC135Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 135mV$, $V_{IL(AC)} = V_{REF(DC)} - 135mV$ DC100Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 100mV$, $V_{IL(DC)} = V_{REF(DC)} - 100mV$																									
		DQS, DQS# Differential Slew Rate																							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ Slew Rate V/ns	4.0	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30			-	-
	0.8	-	-	-	-	-	-	-	-	-	-			-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-36	-76	-30	-60

Note:

1. Cell contents which is '-' are defined as 'not supported'.

Table 66 - Derating values for DDR3-800/1066 t_{DS}/t_{DH} – (AC175) (1.5V)

AC175 Threshold-> $V_{IH(AC)} = V_{REF(DC)} + 175mV$, $V_{IL(AC)} = V_{REF(DC)} - 175mV$																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}
DQ Slew Rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

Table 67 - Derating values for DDR3-800/1066/1333/1600 t_{DS}/t_{DH} – (AC150) (1.5V)

AC150 Threshold-> $V_{IH(AC)} = V_{REF(DC)} + 150mV$, $V_{IL(AC)} = V_{REF(DC)} - 150mV$																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}
DQ Slew Rate V/ns	2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

Table 68 - Derating values for DDR3-800/1066/1333/1600 t_{DS}/t_{DH} – (AC135) (1.5V)

AC150 Threshold-> $V_{IH(AC)} = V_{REF(DC)} + 150mV$, $V_{IL(AC)} = V_{REF(DC)} - 150mV$																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}
DQ Slew Rate V/ns	2.0	68	50	68	50	68	50	-	-	-	-	-	-	-	-	-	-
	1.5	45	34	45	34	45	35	53	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-4	2	-4	10	4	18	12	26	20	-	-	-	-
	0.8	-	-	-	-	3	-10	11	-2	19	6	27	14	35	24	-	-
	0.7	-	-	-	-	-	-	14	-8	22	0	30	8	38	18	46	34
	0.6	-	-	-	-	-	-	-	-	25	-10	33	-2	41	8	49	24
	0.5	-	-	-	-	-	-	-	-	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-26	38	-10

Table 69 - Derating values for DDR3-1866/2133 t_{DS}/t_{DH} – (AC135) (1.5V)

AC135Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 135mV$, $V_{IL(AC)} = V_{REF(DC)} - 135mV$ DC100Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 100mV$, $V_{IL(DC)} = V_{REF(DC)} - 100mV$																							
		DQS, DQS# Differential Slew Rate																					
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ Slew Rate V/ns	4.0	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30			-	-
	0.8	-	-	-	-	-	-	-	-	-	-			-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-36	-76	-30	-60

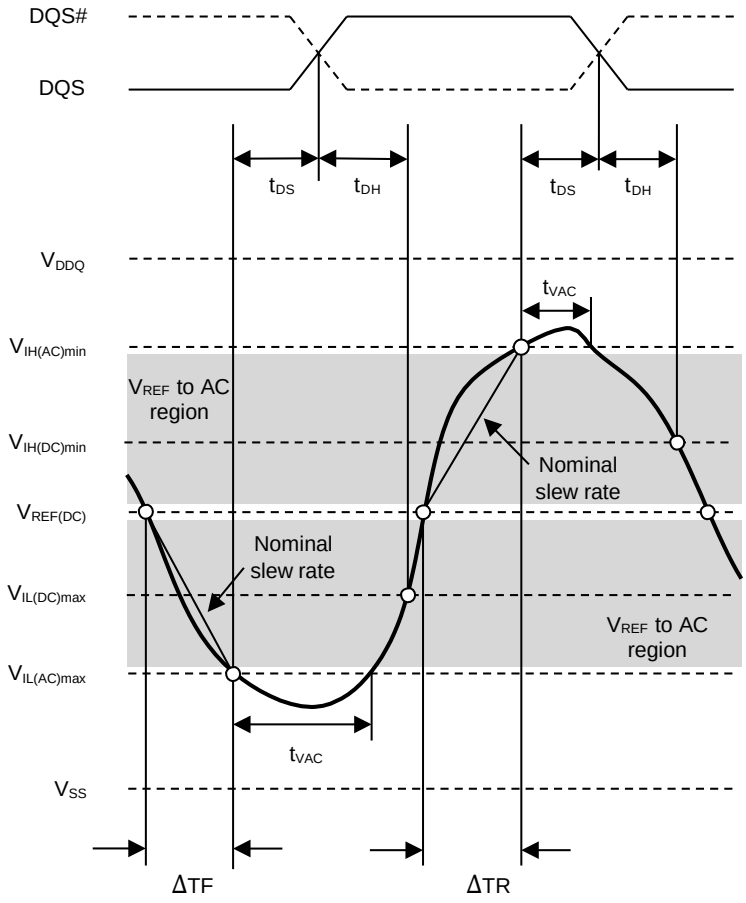
Table 70 - Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid DQ transition

Slew Rate [V/ns]	DDR3 (1.5V)					DDR3L (1.35V)				Unit
	800/1066	800/1066/ 1333/1600	800/1066/ 1333/1600	1866	2133	800/1066	800/1066/ 1333/1600	1866	2133	
	AC175	AC150	AC135			AC160	AC135	AC130	AC130	
>2.0	75	105	113	93	73	165	113	95	73	ps
2.0	57	105	113	93	73	165	113	95	73	ps
1.5	50	80	90	70	50	138	90	73	50	ps
1.0	38	30	45	25	5	85	45	30	5	ps
0.9	34	13	30	Note	Note	67	30	16	Note	ps
0.8	29	Note	11	Note	Note	45	11	Note	Note	ps
0.7	Note	Note	Note	-	-	16	Note	-	-	ps
0.6	Note	Note	Note	-	-	Note	Note	-	-	ps
0.5	Note	Note	Note	-	-	Note	Note	-	-	ps
<0.5	Note	Note	Note	-	-	Note	Note	-	-	ps

Note:

Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

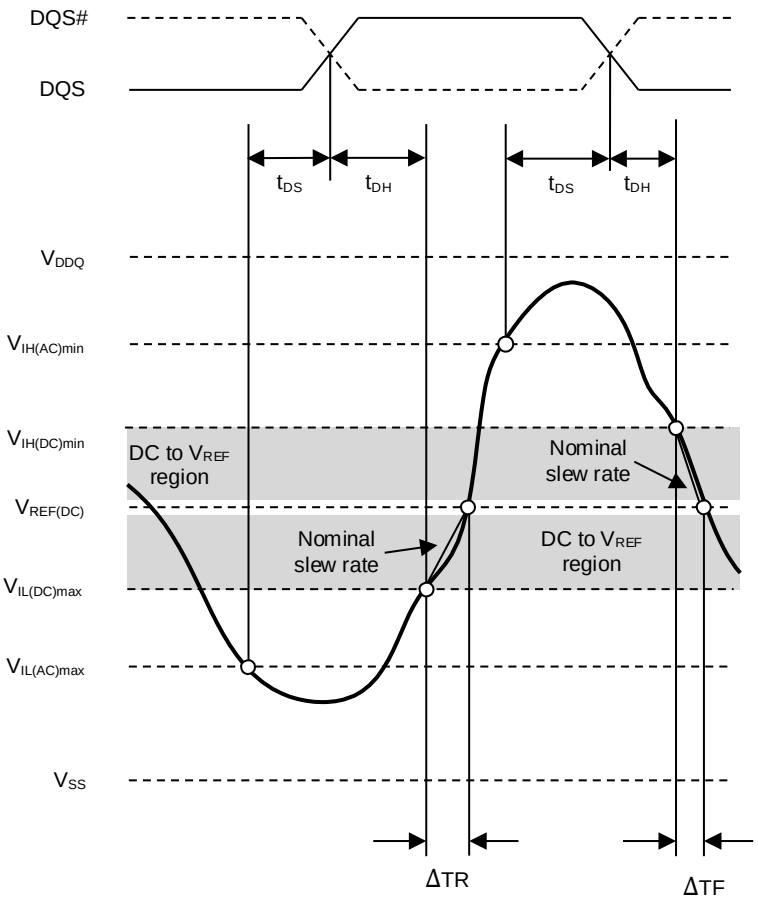
Figure 29 - Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)min} - V_{REF(dc)}}{\Delta TR}$$

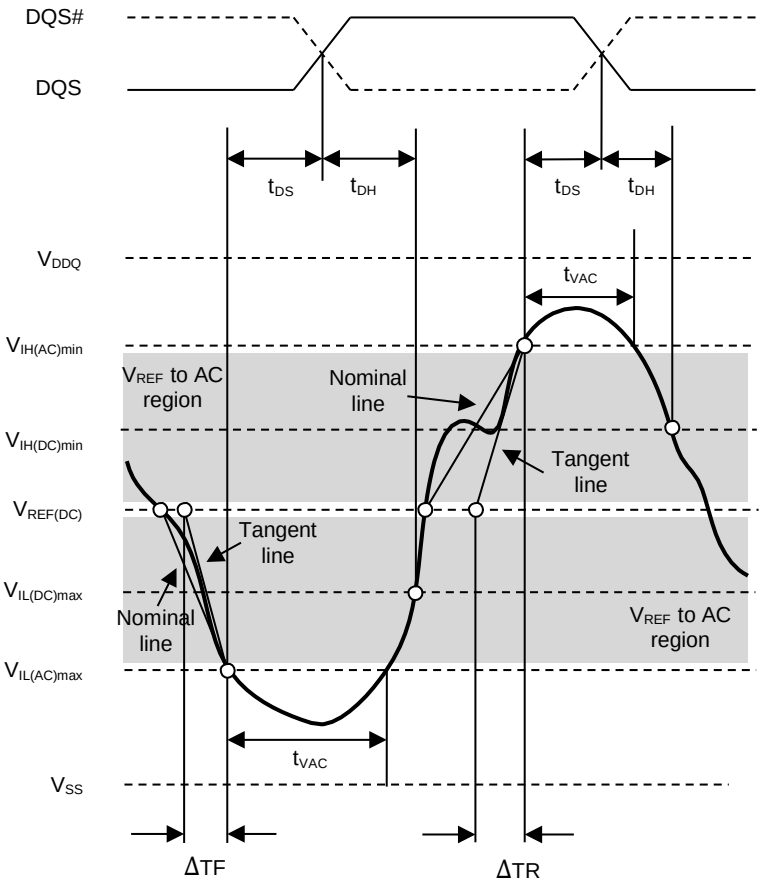
Figure 30 - Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)max}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)min} - V_{REF(dc)}}{\Delta TF}$$

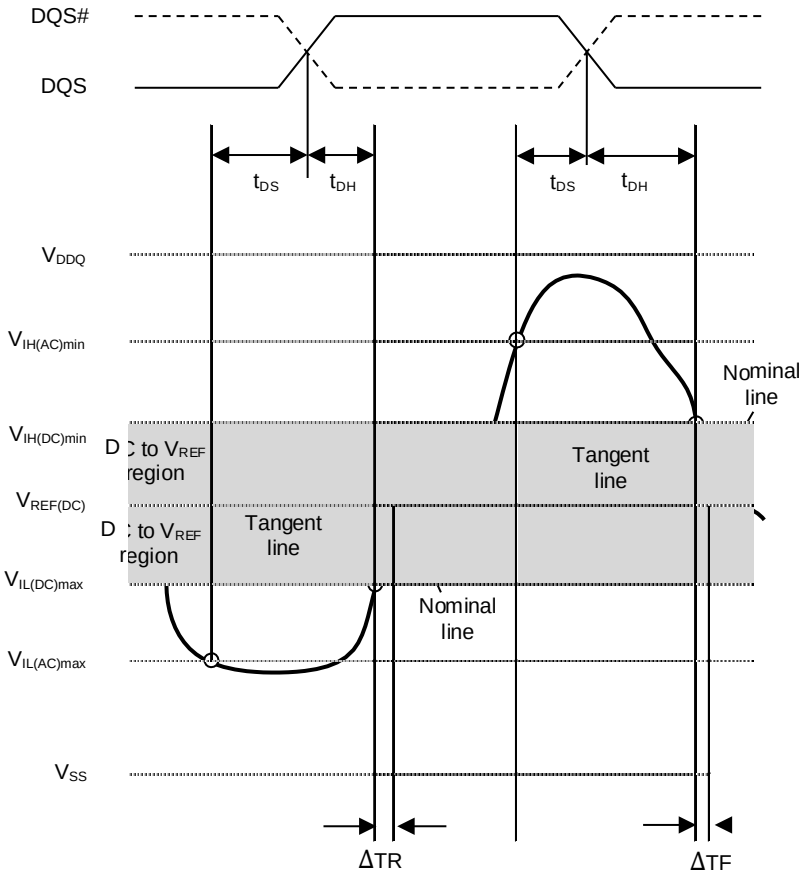
Figure 31 - Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe)



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{IH(ac)min} - V_{REF(dc)}]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{REF(dc)min} - V_{IL(ac)}max]}{\Delta TF}$$

Figure 32 - Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - V_{IL(dc)min}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(dc)min} - V_{REF(dc)}]}{\Delta TF}$$

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