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SCB13H2G800DF

2Gbit DDR3L SDRAM

EU RoHS Compliant Products

Data Sheet

Rev. B

Revision History:		
Date	**Revision**	**Subjects (major changes since last revision)**
2018-11	A	Initial release
2024-05	B	Correcting typo

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Contents

1 Features

The 2Gbit DDR3L SDRAM offers the following key features:

- Density: 2Gbits
- Power Supply
  - VDD,=VDDQ=1.35V(1.283-1.45V)
  - Backward compatible to be backward compatible in 1.5V application.
- Differential bidirectional data strobe
- 8n-bit prefetcharchitecture
- Data rate:
  - 1866Mbps,1600Mbps
- 8 Internal Banks:
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Selfrefreshmode
- Pre-charge: auto pre-charge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - 7.8us at 0℃≤Tc≤+85℃
  - 3.9us at 85℃≤Tc≤+95℃
- Timing –cycle time
  - 1.07ns @CL=13(DDR3-1866)
  - 1.25ns @CL=11(DDR3-1600)
- Operating case temperature range:
  - C: Commercial Tc =0℃ to +95℃
- Configuration
  - 256Meg x8
- Package
  - 78Ball FBGA
- Green Product
  - Pb-free
  - RoHS

2 Product List

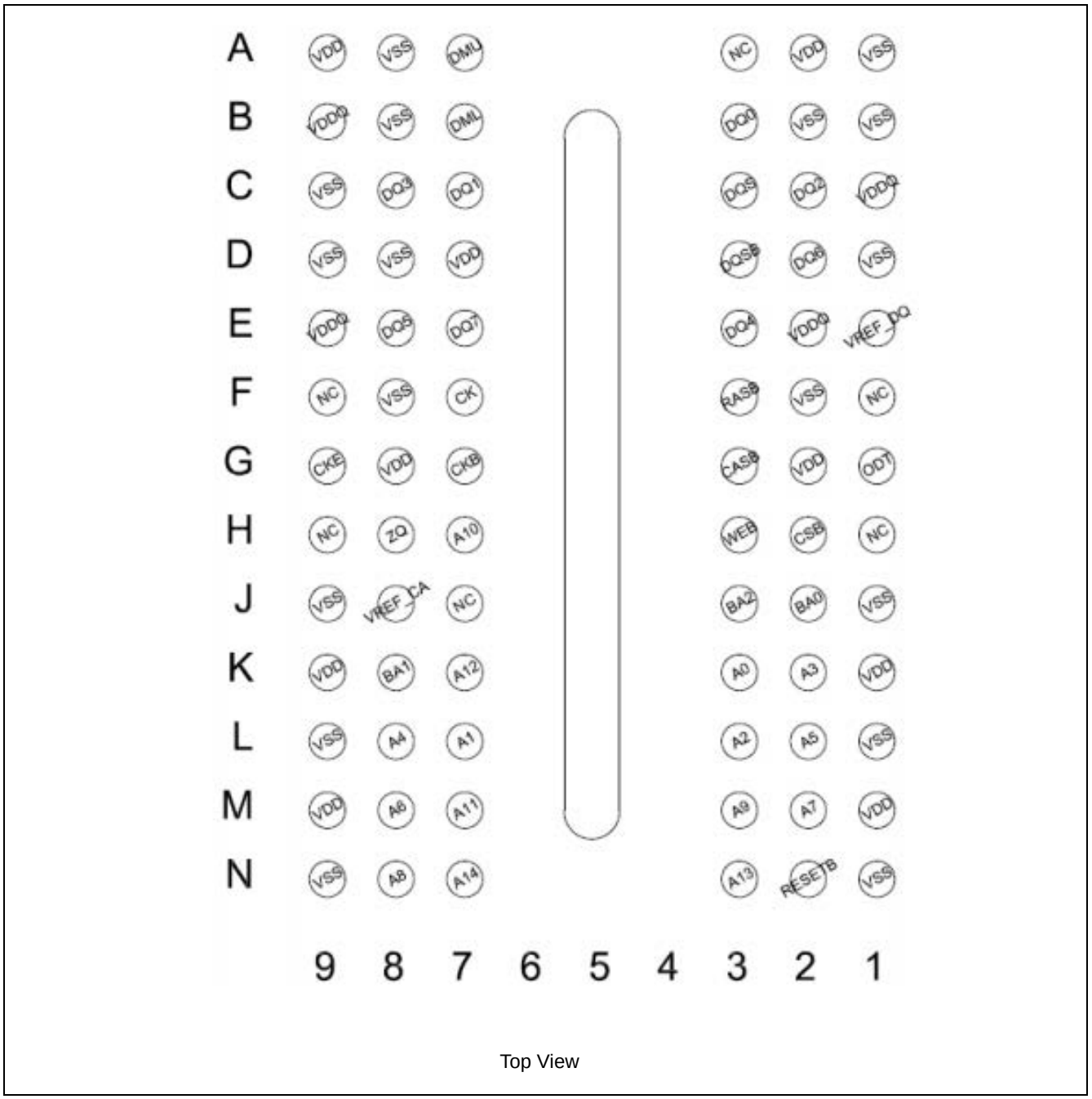
Table 1 shows all possible products within the 2Gbit DDR3L SDRAM component generation.

Table 1 - Ordering Information for 2Gbit DDR3L Component

UniIC Part Number	Max. Clock Frequency	CAS-RCD-RP Latencies	Speed Sort Name	Package
2Gbit DDR3L SDRAM Components in × 8 Organization (256M × 8)				
SCB13H2G800DF-11M	1866MHz	13-13-13	DDR3–1866M	PG-FBGA-78
SCB13H2G800DF-13K	1600 MHz	11-11-11	DDR3-1600K	PG-FBGA-78

3 Ball configuration

Figure 1 - Ball out for 256 Mb ×8 Components (FBGA-78)



Top View

4 Ball Description

Table 2 - Input / Output Signal Functional Description

Symbol	Type	Function
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE	Input	**Clock Enable:** CKE High activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (active row in any bank). CKE is asynchronous for Self-Refresh exit. After V_{REFCA} and V_{REFDQ} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained High throughout read and write accesses. Input buffers, excluding CK, CK#, ODT, CKE and RESET# are disabled during Power-down. Input buffers, excluding CKE and RESET are disabled during self refresh.
CS#	Input	**Chip Select:** All commands are masked when CS# is registered High. CS# provides for external Rank selection on systems with multiple ranks. CS# is considered part of the command code.
RAS#, CAS#, WE#	Input	**Command Inputs: RAS#**, CAS# and WE# (along with CS#) define the command being entered.
ODT	Input	**On-Die Termination:** ODT (registered High) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU and DML signal for ×16 configurations. The ODT signal will be ignored if the Mode Register MR1 and MR2 are programmed to disable ODT and during Self Refresh.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	**Bank Address Inputs:** Define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a mode register set cycle.
A[14:13], A12, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the

Symbol	Type	Function
		op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
DQ(DQL0~7), (DQU0~7)	Input/ Output	**Data Input/Output:** Bi-directional data bus.
DQSL,DQSL# DQSU, DQSU#	Input/ Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQSL and DQSU are paired with differential signals DQSL# and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
RESET#	Input	**Active Low Asynchronous Reset:** Reset is active when RESET# is Low, and inactive when RESET# is High. RESET# must be High during normal operation. RESET# is a CMOS rail to rail signal with DC High and Low are 80% and 20% of V_{DD}, RESET# active is destructive to data contents.
NC	—	**No Connect:** no internal electrical connection is present
V_{DDQ}	Supply	**DQ Power Supply:** 1.35V, 1.283–1.45V operational; compatible to 1.5V operation
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 1.35V, 1.283–1.45V operational; compatible to 1.5V operation
V_{SS}	Supply	**Ground**
V_{REFDQ}	Supply	**Reference Voltage for DQ**
V_{REFCA}	Supply	**Reference Voltage for Command and Address inputs**
ZQ	Supply	Reference ball for ZQ calibration

5 Electrical Specifications

Table 3 - IDD & IDDQ Specification

Parameter	Symbol	DDR3L-1600	DDR3L-1866	Unit	
Operating current 0: One bank ACTIVATE-to-PRECHARGE	IDD0	47	49	mA	1, 2
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	IDD1	61	64	mA	1, 2
Precharge power-down current: Slow exit	IDD2P0	8	8	mA	1, 2
Precharge power-down current: Fast exit	IDD2P1	14	16	mA	1, 2
Precharge quiet standby current	IDD2Q	24	26	mA	1, 2
Precharge standby current	IDD2N	24	26	mA	1, 2
Precharge standby ODT current	IDD2NT	28	30	mA	1,2
Active power-down current	IDD3P	26	28	mA	1, 2
Active standby current	IDD3N	30	32	mA	1, 2
Burst read operating current	IDD4R	95	105	mA	1, 2
Burst write operating current	IDD4W	95	105	mA	1, 2
Burst refresh current	IDD5B	235	242	mA	1, 2,3
Room temperature self refresh	IDD6	12	12	mA	2,4
Extended temperature self refresh	IDD6E	16	16	mA	1, 2
All banks interleaved read current	IDD7	140	140	mA	1, 2
Reset current	IDD8	IDD2P + 2mA	IDD2P + 2mA	mA	

Notes:

1. T_C = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
3. Restricted to T_C (MAX) = 85°C.
4. T_C = 85°C; ASR and ODT are disabled; SRT is enabled.
5. The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range 0°C ≤ T_C ≤ +85°C:
   a. 5a. When T_C < 0°C: I_{DD2P0}, I_{DD2P1} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6}, I_{DD6ET} and I_{DD7} must be derated by 7%.
   b. 5b. When T_C > 85°C: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5B} must be derated by 2%; I_{DD2Px} must be derated by 30%.

6 Speed Bin

Table 4 - DDR3-1600 Speed Bins

Speed Bin			**DDR3-1600**		**Unit**	**Note**
CL-nRCD-nRP			**11-11-11**		**Unit**	**Note**
Parameter		**Symbol**	**Min.**	**Max.**		
Internal read command to first data		tAA	13.75	-	ns	
ACT to internal read or write delay time		tRCD	13.75	-	ns	
PRE command period		tRP	13.75	-	ns	
ACT to PRE command period		tRAS	35	9*tREFI	ns	
ACT to ACT or REF command period		tRC	48.75		ns	
CL=5	CWL=5	tCK(avg)	3.0	3.3	ns	
	CWL=6,7,8	tCK(avg)	Reserved		ns	
CL=6	CWL=5	tCK(avg)	2.5	3.3	ns	
	CWL=6	tCK(avg)	Reserved			
	CWL=7,8	tCK(avg)	Reserved		ns	
CL=7,8	CWL=5	tCK(avg)	Reserved		ns	
	CWL=6	tCK(avg)	1.875	＜2.5	ns	
	CWL=7	tCK(avg)	Reserved		ns	
	CWL=8	tCK(avg)	Reserved		ns	
CL=9,10	CWL=5,6	tCK(avg)	Reserved		ns	
	CWL=7	tCK(avg)	1.5	＜1.875	ns	
	CWL=8	tCK(avg)	Reserved		ns	
CL=11	CWL=5,6,7	tCK(avg)	Reserved		Ns	
	CWL=8	tCK(avg)	1.25	＜1.5	ns	
Supported CL setting			5,6,7,8,9,10,11		CK	13,14
Supported CWL setting			5,6,7,8		nCK	

Table 5 - DDR3-1866 Speed Bins

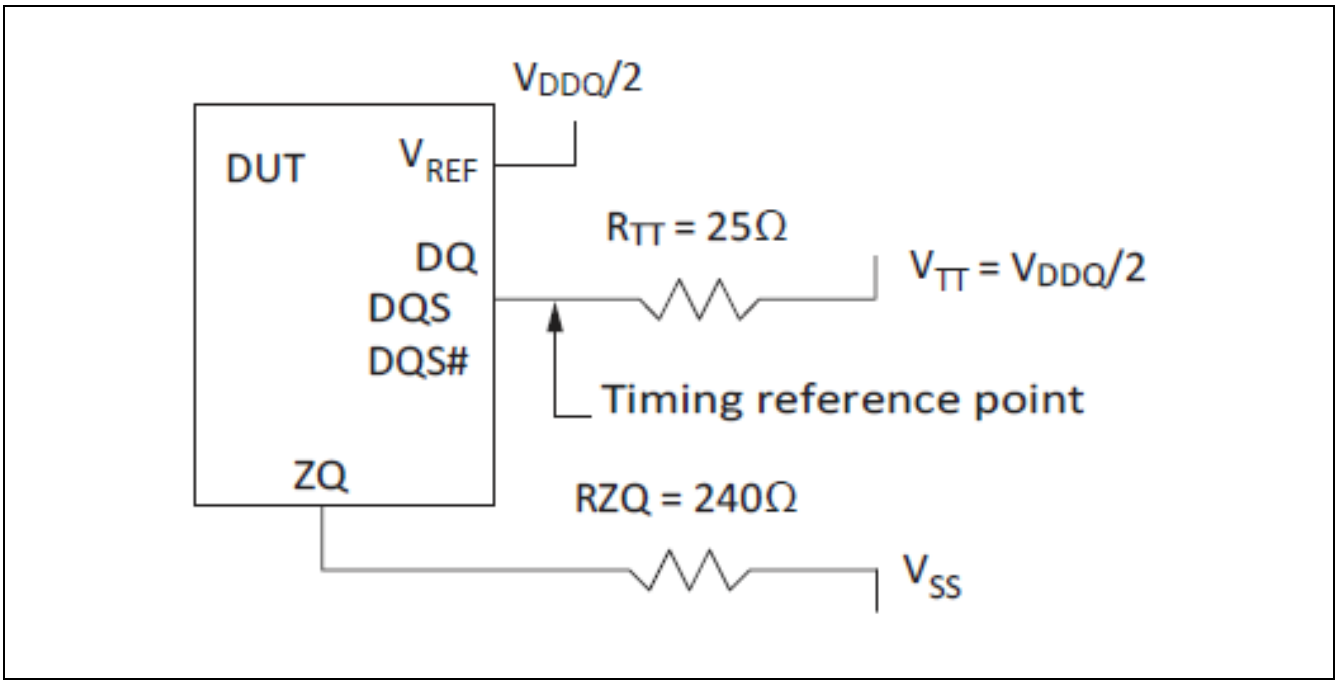
Speed Bin			DDR3-1866		Unit	Note
CL-nRCD-nRP			13-13-13		Unit	Note
Parameter		Symbol	Min.	Max.		
Internal read command to first data		tAA	13.91	-	ns	
ACT to internal read or write delay time		tRCD	13.91	-	ns	
PRE command period		tRP	13.91	-	ns	
ACT to PRE command period		tRAS	34	9*tREFI	ns	
ACT to ACT or REF command period		tRC	47.91		ns	
CL=5	CWL=5	tCK(avg)	3.0	3.3	ns	
	CWL=6,7,8,9	tCK(avg)	Reserved		ns	
CL=6	CWL=5	tCK(avg)	2.5	3.3	ns	
	CWL=6,7,8,9	tCK(avg)	Reserved		ns	
CL=7	CWL=5,7,8,9	tCK(avg)	Reserved		ns	
	CWL=6	tCK(avg)	1.875	＜2.5	ns	
CL=8	CWL=5,8,9	tCK(avg)	Reserved		ns	
	CWL=6	tCK(avg)	1.875	＜2.5	ns	
	CWL=7	tCK(avg)	Reserved		ns	
CL=9	CWL=5,6,8,9	tCK(avg)	Reserved		ns	
	CWL=7	tCK(avg)	1.5	＜1.875	ns	
CL=10	CWL=5,6,9	tCK(avg)	Reserved		Ns	
	CWL=7	tCK(avg)	1.5	＜1.875		
	CWL=8	tCK(avg)	Reserved		ns	
CL=11	CWL=5,6,7	tCK(avg)	Reserved		ns	
	CWL=8	tCK(avg)	1.25	＜1.5	ns	
	CWL=9	tCK(avg)	Reserved		ns	
CL=12	CWL=5,6,7,9	tCK(avg)	Reserved		ns	
	CWL=9	tCK(avg)	Reserved		ns	
CL=13	CWL=5,6,7,8	tCK(avg)	Reserved		ns	
	CWL=9	tCK(avg)	Reserved		ns	
Supported CL setting			5,6,7,8,9,10,11,13		CK	
Supported CWL setting			5,6,7,8,9		CK	

7 Electrical Characteristics & Timing

7.1 Reference Load for AC Timing and Output Slew Rate

Figure 2 represents the effective reference load of 25 Ω used in defining the relevant timing parameters of the device as well as for output slew rate measurements. It is not intended as either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics

Figure 2 - Reference Load for AC Timings and Output Slew Rates



7.2 Timing Parameters by Speed Grade

Table 6 - AC Timing parameters

Parameter		Symbol	DDR3L-1600 Min	DDR3L-1600 Max	Unit	Notes
Clock Timing						
Clock period average: DLL disable mode	$T_C \leq 85°C$	^tCK (DLL_DIS)	8	7800	ns	9, 42
	T_C = >85°C to 95°C		8	3900	ns	42
Clock period average: DLL enable mode		^tCK (AVG)			ns	10, 11
High pulse width average		^tCH (AVG)	0.47	0.53	CK	12
Low pulse width average		^tCL (AVG)	0.47	0.53	CK	12
Clock period jitter	DLL locked	^tJITper	–70	70	ps	13
	DLL locking	$^tJITper,lck$	–60	60	ps	13
Clock absolute period		^tCK (ABS)	MIN = tCK (AVG) MIN + tJITper MIN; MAX = tCK (AVG) MAX + tJITper		ps	
Clock absolute high pulse width		^tCH (ABS)	0.43	–	^tCK (AVG)	14
Clock absolute low pulse width		^tCL (ABS)	0.43	–	^tCK (AVG)	15
Cycle-to-cycle jitter	DLL locked	^tJITcc	140		ps	16
	DLL locking	$^tJITcc,lck$	120		ps	16
Cumulative error across	2 cycles	$^tERR2per$	–103	103	ps	17
	3 cycles	$^tERR3per$	–122	122	ps	17
	4 cycles	$^tERR4per$	–136	136	ps	17
	5 cycles	$^tERR5per$	–147	147	ps	17
	6 cycles	$^tERR6per$	–155	155	ps	17
	7 cycles	$^tERR7per$	–163	163	ps	17
	8 cycles	$^tERR8per$	–169	169	ps	17
	9 cycles	$^tERR9per$	–175	175	ps	17
	10 cycles	$^tERR10per$	–180	180	ps	17
	11 cycles	$^tERR11per$	–184	184	ps	17
	12 cycles	$^tERR12per$	–188	188	ps	17
	n = 13, 14 . . . 49, 50 cycles	$^tERRnper$	tERRnper MIN = (1 + 0.68ln[n]) × tJITper MIN tERRnper MAX = (1 + 0.68ln[n]) × tJITper MAX		ps	17

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
DQ Input Timing						
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC160)	–	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC135)	25	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		160	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	^{t}DH (DC90)	55	–	ps	18, 19
	V_{REF} @ 1 V/ns		145	–	ps	19, 20
Minimum data pulse width		^{t}DIPW	360	–	ps	41
DQ Output Timing						
DQS, DQS# to DQ skew, per access		^{t}DQSQ	–	100	ps	
DQ output hold time from DQS, DQS#		^{t}QH	0.38	–	^{t}CK (AVG)	21
DQ Low-Z time from CK, CKB		^{t}LZDQ	–450	225	ps	22, 23
DQ High-Z time from CK, CKB		^{t}HZDQ	–	225	ps	22, 23
DQ Strobe Input Timing						
DQS, DQS# rising to CK, CKB rising		^{t}DQSS	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		^{t}DQSL	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		^{t}DQSH	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CKB rising		^{t}DSS	0.18	–	CK	25
DQS, DQS# falling hold from CK, CKB rising		^{t}DSH	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		^{t}WPRE	0.9	–	CK	
DQS, DQS# differential WRITE postamble		^{t}WPST	0.3	–	CK	
DQ Strobe Output Timing						
DQS, DQS# rising to/from rising CK, CKB		^{t}DQSCK	–225	225	ps	23
DQS, DQS# rising to/from rising CK, CKB		^{t}DQSCK	–225	225	ps	23
DQS, DQS# rising to/from rising CK, CKB when DLL is disabled		^{t}DQSCK (DLL_DIS)	1	10	ns	26
DQS, DQS# differential output high time		^{t}QSH	0.40	–	CK	21
DQS, DQS# differential output low time		^{t}QSL	0.40	–	CK	21

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
DQS, DQS# Low-Z time (RL - 1)		tLZDQS	–450	225	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		tHZDQS	–	225	ps	22, 23
DQS, DQS# differential READ preamble		tRPRE	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		tRPST	0.3	Note 27	CK	23, 27
Command and Address Timing						
DLL locking time		tDLLK	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	tIS (AC160)	60	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		220	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	tIS (AC135)	185	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		320	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	tIH (DC90	130	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		220	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		tIPW	560	–	ps	41
ACTIVATE to internal READ or WRITE delay		tRCD	See Speed Bin Tables for tRCD		ns	31
PRECHARGE command period		tRP	See Speed Bin Tables for tRP		ns	31
ACTIVATE-to-PRECHARGE command period		tRAS	See Speed Bin Tables for tRAS		ns	31, 32
ACTIVATE-to-ACTIVATE command period		tRC	See Speed Bin Tables for tRC		ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	X8 (1KB page size)	tRRD	MIN = greater of 4CK or 6ns		CK	31
Four ACTIVATE windows	X8 (1KB page size)	tFAW	30	–	ns	31
					ns	31
Write recovery time		tWR	MIN = 15ns; MAX = N/A		ns	31, 32, 33,34
Delay from start of internal WRITE transaction to internal READ command		tWTR	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 34
READ-to-PRECHARGE time		tRTP	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 32

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
CASB-to-CASB command delay		tCCD	MIN = 4CK; MAX = N/A		CK	
Auto precharge write recovery + precharge time		tDAL	MIN = WR + tRP/tCK (AVG); MAX = N/A		CK	
MODE REGISTER SET command cycle time		tMRD	MIN = 4CK; MAX = N/A		CK	
MODE REGISTER SET command update delay		tMOD	MIN = greater of 12CK or 15ns; MAX = N/A		CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		tMPRR	MIN = 1CK; MAX = N/A		CK	
Calibration Timing						
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	512	–	CK	
	Normal operation	tZQoper	256	–	CK	
ZQCS command: Short calibration time		tZQCS	64	–	CK	
Initialization and Reset Timing						
Exit reset from CKE HIGH to a valid command		tXPR	MIN = greater of 5CK or tRFC + 10ns; MAX = N/A		CK	
Begin power supply ramp to power supplies stable		tVDDPR	MIN = N/A; MAX = 200		ms	
RESET# LOW to power supplies stable		tRPS	MIN = 0; MAX = 200		ms	
RESET# LOW to I/O and R_{TT} High-Z		tIOZ	MIN = N/A; MAX = 20		ns	35
Refresh Timing						
REFRESH-to-ACTIVATE or REFRESH command period		tRFC – 1Gb			ns	
		tRFC – 2Gb	MIN = 260; MAX = 70,200		ns	
		tRFC – 4Gb			ns	
		tRFC – 8Gb			ns	
Maximum refresh period	$T_C \leq 85°C$	–	64 (1X)		ms	36
	$T_C > 85°C$		32 (2X)		ms	36
Maximum average periodic refresh	$T_C \leq 85°C$	tREFI	7.8 (64ms/8192)		µs	36
	$T_C > 85°C$		3.9 (32ms/8192)		µs	36
Self Refresh Timing						
Exit self refresh to commands not requiring a locked DLL		tXS	MIN = greater of 5CK or tRFC + 10ns; MAX = N/A		CK	

Parameter	Symbol	DDR3L-1600 Min	DDR3L-1600 Max	Unit	Notes
Exit self refresh to commands requiring a locked DLL	tXSDLL	MIN = tDLLK (MIN); MAX = N/A		CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing	tCKESR	MIN = tCKE (MIN) + CK; MAX = N/A		CK	
Valid clocks after self refresh entry or power-down entry	tCKSRE	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Valid clocks before self refresh exit, power-down exit, or reset exit	tCKSRX	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Power-Down Timing					
CKE MIN pulse width	tCKE (MIN)	Greater of 3CK or 5ns		CK	
Command pass disable delay	tCPDED	MIN = 1; MAX = N/A		CK	
Power-down entry to power-down exit timing	tPD	MIN = tCKE (MIN); MAX = 9 * tREFI		CK	
Begin power-down period prior to CKE registered HIGH	tANPD	WL - 1CK		CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time		CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	tANPD + tXPDLL		CK	
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry	tACTPDEN	MIN = 1		CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	tPRPDEN	MIN = 1		CK	
REFRESH command to power-down entry	tREFPDEN	MIN = 1		CK	37
MRS command to power-down entry	tMRSPDEN	MIN = tMOD (MIN)		CK	
READ/READ with auto precharge command to power-down entry	tRDPDEN	MIN = RL + 4 + 1		CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRPDEN	MIN = WL + 4 + tWR/tCK (AVG)	CK	
	BC4MRS	tWRPDEN	MIN = WL + 2 + tWR/tCK (AVG)	CK	

Parameter		Symbol	DDR3L-1600 Min	DDR3L-1600 Max	Unit	Notes
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAP-DEN	MIN = WL + 4 + WR + 1		CK	
	BC4MRS	^{t}WRAP-DEN	MIN = WL + 2 + WR + 1		CK	
Power-Down Exit Timing						
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 6ns; MAX = N/A		CK	
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = N/A		CK	28
ODT Timing						
R_{TT} synchronous turn-on delay		ODTLon	CWL + AL - 2CK		CK	38
R_{TT} synchronous turn-off delay		ODTLoff	CWL + AL - 2CK		CK	40
R_{TT} turn-on from ODTL on reference		^{t}AON	-225	225	ps	23, 38
R_{TT} turn-off from ODTL off reference		^{t}AOF	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	MIN = 2; MAX = 8.5		ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		^{t}AOFPD	MIN = 2; MAX = 8.5		ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A		CK	
ODT HIGH time without WRITE command or with WRITE command and BC4		ODTH4	MIN = 4; MAX = N/A		CK	
Dynamic ODT Timing						
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew		ODTLcnw	WL - 2CK		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4		ODTLcwn4	4CK + ODTLoff		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8		ODTLcwn8	6CK + ODTLoff		CK	
R_{TT} dynamic change skew		^{t}ADC	0.3	0.7	CK	39
Write Leveling Timing						
First DQS, DQS# rising edge		^{t}WLMRD	40	-	CK	
DQS, DQS# delay		^{t}WLDQSEN	25	-	CK	
Write leveling setup from rising CK, CKB crossing to rising DQS, DQS# crossing		^{t}WLS	165	-	ps	

Parameter	Symbol	DDR3L-1600		Unit	Notes
		Min	Max		
Write leveling hold from rising DQS, DQS# crossing to rising CK, CKB crossing	^{t}WLH	165	–	ps	
Write leveling output delay	^{t}WLO	0	7.5	ns	
Write leveling output error	^{t}WLOE	0	2	ns	

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
Clock Timing						
Clock period average: DLL disable mode	T_C = 0°C to 85°C	^{t}CK (DLL_DIS)	8	7800	ns	9, 42
	T_C = >85°C to 95°C		8	3900	ns	42
Clock period average: DLL enable mode		^{t}CK (AVG)	See Speed Bin Tables for ^{t}CK range allowed ns			10, 11
High pulse width average		^{t}CH (AVG)	0.47	0.53	CK	12
Low pulse width average		^{t}CL (AVG)	0.47	0.53	CK	12
Clock period jitter	DLL locked	^{t}JITper	–60	60	ps	13
	DLL locking	^{t}JITper,lck	–50	50	ps	13
Clock absolute period		^{t}CK (ABS)	MIN = ^{t}CK (AVG) MIN + ^{t}JITper MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITper MAX ps			
Clock absolute high pulse width		^{t}CH (ABS)	0.43	–	^{t}CK (AVG)	14
Clock absolute low pulse width		^{t}CL (ABS)	0.43	–	^{t}CK (AVG)	15
Cycle-to-cycle jitter	DLL locked	^{t}JITcc	120		ps	16
	DLL locking	^{t}JITcc,lck	100		ps	16
Cumulative error across	2 cycles	^{t}ERR2per	–88	88	ps	17
	3 cycles	^{t}ERR3per	–105	105	ps	17
	4 cycles	^{t}ERR4per	–117	117	ps	17
	5 cycles	^{t}ERR5per	–126	126	ps	17
	6 cycles	^{t}ERR6per	–133	133	ps	17
	7 cycles	^{t}ERR7per	–139	139	ps	17
	8 cycles	^{t}ERR8per	–145	145	ps	17
	9 cycles	^{t}ERR9per	–150	150	ps	17
	10 cycles	^{t}ERR10per	–154	154	ps	17
	11 cycles	^{t}ERR11per	–158	158	ps	17
	12 cycles	^{t}ERR12per	–161	161	ps	17
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*]) × ^{t}JITper MIN ^{t}ERR*n*per MAX = (1 + 0.68ln[*n*]) × ^{t}JITper MAX		ps	17
DQ Input Timing						
Data setup time to DQS, DQS#	Base (specification) @ 2 V/ns	^{t}DS (AC130)	70	–	ps	18, 19
	V_{REF} @ 2 V/ns		135	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification) @ 2 V/ns	^{t}DH (DC90)	75	–	ps	18, 19
	V_{REF} @ 2 V/ns		110	–	ps	19, 20
Minimum data pulse width		^{t}DIPW	320	–	ps	41
DQ Output Timing						
DQS, DQS# to DQ skew, per access		^{t}DQSQ	–	85	ps	
DQ output hold time from DQS, DQS#		^{t}QH	0.38	–	^{t}CK (AVG)	21
DQ Low-Z time from CK, CKB		^{t}LZDQ	–390	195	ps	22, 23
DQ High-Z time from CK, CKB		^{t}HZDQ	–	195	ps	22, 23
DQ Strobe Input Timing						
DQS, DQS# rising to CK, CKB rising		^{t}DQSS	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		^{t}DQSL	0.45	0.55	CK	

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
DQS, DQS# differential input high pulse width		tDQSH	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CKB rising		tDSS	0.18	_	CK	25
DQS, DQS# falling hold from CK, CKB rising		tDSH	0.18	_	CK	25
DQS, DQS# differential WRITE preamble		tWPRE	0.9	_	CK	
DQS, DQS# differential WRITE postamble		tWPST	0.3	_	CK	
DQ Strobe Output Timing						
DQS, DQS# rising to/from rising CK, CKB		tDQSCK	–195	195	ps	23
DQS, DQS# rising to/from rising CK, CKB when DLL is disabled		tDQSCK (DLL_DIS)	1	10	ns	26
DQS, DQS# differential output high time		tQSH	0.40	_	CK	21
DQS, DQS# differential output low time		tQSL	0.40	_	CK	21
DQS, DQS# Low-Z time (RL - 1)		tLZDQS	–390	195	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		tHZDQS	–	195	ps	22, 23
DQS, DQS# differential READ preamble		tRPRE	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		tRPST	0.3	Note 27	CK	23, 27
Command and Address Timing						
DLL locking time		tDLLK	512	_	CK	28
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	tIS (AC135)	65	_	ps	29, 30, 44
	V_{REF} @ 1 V/ns		200	_	ps	20, 30
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	tIS (AC125)	150	_	ps	29, 30, 44
	V_{REF} @ 1 V/ns		275	_	ps	20, 30
CTRL, CMD, ADDR hold from CK,CKB	Base (specification)	tIH (DC90)	110	_	ps	29, 30
	V_{REF} @ 1 V/ns		200	_	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		tIPW	535	_	ps	41
ACTIVATE to internal READ or WRITE delay		tRCD	See Speed Bin Tables for tRCD		ns	31

PRECHARGE command period	tRP	See Speed Bin Tables for tRP	ns	31
ACTIVATE-to-PRECHARGE command period	tRAS	See Speed Bin Tables for tRAS	ns	31, 32
ACTIVATE-to-ACTIVATE command period	tRC	See Speed Bin Tables for tRC	ns	31, 43

Parameter		Symbol	DDR3L-1866 Min	DDR3L-1866 Max	Unit	Notes
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	^{t}RRD	MIN = greater of 4CK or 5ns		CK	31
	2KB page size		MIN = greater of 4CK or 6ns		CK	31
Four ACTIVATE windows	1KB page size	^{t}FAW	27	–	ns	31
	2KB page size		35	–	ns	31
Write recovery time		^{t}WR	MIN = 15ns; MAX = N/A		ns	31, 32, 33
Delay from start of internal WRITE transaction to internal READ command		^{t}WTR	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 34
READ-to-PRECHARGE time		^{t}RTP	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 32
CASB-to-CASB command delay		^{t}CCD	MIN = 4CK; MAX = N/A		CK	
Auto precharge write recovery + precharge time		^{t}DAL	MIN = WR + ^{t}RP/^{t}CK (AVG); MAX = N/A		CK	
MODE REGISTER SET command cycle time		^{t}MRD	MIN = 4CK; MAX = N/A		CK	
MODE REGISTER SET command update delay		^{t}MOD	MIN = greater of 12CK or 15ns; MAX = N/A		CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^{t}MPRR	MIN = 1CK; MAX = N/A		CK	
Calibration Timing						
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	MIN = N/A MAX = MAX(512nCK, 640ns)		CK	
	Normal operation	^{t}ZQoper	MIN = N/A MAX = max(256nCK, 320ns)		CK	
ZQCS command: Short calibration time			MIN = N/A MAX = max(64nCK, 80ns) ^{t}ZQCS		CK	
Initialization and Reset Timing						
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A		CK	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200		ms	
RESET# LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 200		ms	
RESET# LOW to I/O and R_{TT} High-Z		^{t}IOZ	MIN = N/A; MAX = 20		ns	35
Refresh Timing						

Parameter		Symbol	DDR3L-1866 Min	DDR3L-1866 Max	Unit	Notes
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC – 1Gb			ns	
		^{t}RFC – 2Gb	MIN = 260; MAX = 70,200		ns	
		^{t}RFC – 4Gb			ns	
		^{t}RFC – 8Gb			ns	
Maximum refresh period	$T_C \leq 85°C$	–	64 (1X)		ms	36
	$T_C > 85°C$		32 (2X)		ms	36
Maximum average periodic refresh	$T_C \leq 85°C$	^{t}REFI	7.8 (64ms/8192)		µs	36
	$T_C > 85°C$		3.9 (32ms/8192)		µs	36
Self Refresh Timing						
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A		CK	
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN); MAX = N/A		CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + CK; MAX = N/A		CK	
Valid clocks after self refresh entry or power-down entry		^{t}CKSRE	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	MIN = greater of 5CK or 10ns; MAX = N/A		CK	

Power-Down Timing				
CKE MIN pulse width	^{t}CKE (MIN)	Greater of 3CK or 5ns	CK	
Command pass disable delay	^{t}CPDED	MIN = 2; MAX = N/A	CK	
Power-down entry to power-down exit timing	^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 * tREFI	CK	
Begin power-down period prior to CKE registered HIGH	^{t}ANPD	WL - 1CK	CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time	CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	^{t}ANPD + ^{t}XPDLL	CK	

Power-Down Entry Minimum Timing								
Parameter		Symbol	DDR3L-1866			Unit	Notes
			Min		Max		
ACTIVATE command to power-down entry		^{t}ACTPDEN	MIN = 2			CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	MIN = 2			CK	
REFRESH command to power-down entry		^{t}REFPDEN	MIN = 2			CK	37
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)			CK	
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1			CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)			CK	
	BC4MRS	^{t}WRPDEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)			CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAPDEN	MIN = WL + 4 + WR + 1			CK	
	BC4MRS	^{t}WRAPDEN	MIN = WL + 2 + WR + 1			CK	
Power-Down Exit Timing							
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 6ns; MAX = N/A			CK	
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = N/A			CK	28
ODT Timing							
R_{TT} synchronous turn-on delay		ODTL on	CWL + AL - 2CK			CK	38
R_{TT} synchronous turn-off delay		ODTL off	CWL + AL - 2CK			CK	40
R_{TT} turn-on from ODTL on reference		^{t}AON	–195	195	–180	180	ps	23, 38
R_{TT} turn-off from ODTL off reference		^{t}AOF	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	MIN = 2; MAX = 8.5			ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		^{t}AOFPD	MIN = 2; MAX = 8.5			ns	40

ODT HIGH time with WRITE command and BL8	ODTH8	MIN = 6; MAX = N/A	CK	

Parameter	Symbol	DDR3L-1866		Unit	Notes
		Min	Max		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = N/A		CK	
Dynamic ODT Timing					
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew	ODTLcnw	WL - 2CK		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4	ODTLcwn4	4CK + ODTLoff		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8	ODTLcwn8	6CK + ODTLoff		CK	
R_{TT} dynamic change skew	^{t}ADC	0.3	0.7	CK	39
Write Leveling Timing					
First DQS, DQS# rising edge	^{t}WLMRD	40	–	CK	
DQS, DQS# delay	^{t}WLDQSEN	25	–	CK	
Write leveling setup from rising CK, CKB crossing to rising DQS, DQS# crossing	^{t}WLS	140	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CKB crossing	^{t}WLH	140	–	ps	
Write leveling output delay	^{t}WLO	0	7.5	ns	
Write leveling output error	^{t}WLOE	0	2	ns	

Notes:

1. AC timing parameters are valid from specified T_C MIN to T_C MAX values.
2. All voltages are referenced to V_{SS}.
3. Output timings are only valid for R_{ON34} output buffer selection.
4. The unit $_{t}$CK (AVG) represents the actual $_{t}$CK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environ- ment, but input timing is still referenced to V_{REF} (except $_{t}$IS, $_{t}$IH, $_{t}$DS, and $_{t}$DH use the AC/DC trip points and CK, CKB and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs (DQs are at 2V/ns for DDR3-1866) and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
6. All timings that use time-based values (ns, μs, ms) should use $_{t}$CK (AVG) to determine the correct number of clocks uses CK or $_{t}$CK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQSdiff refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CKB differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is V_{DDQ}/2 for single-ended signals and the crossing point for differential signals.
9. When operating in DLL disable mode, PTC does not warrant compliance with normal mode timings or functionality.
10. The clock's $_{t}$CK (AVG) is the average clock over any 200 consecutive clocks and $_{t}$CK(AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of $_{t}$CK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below $_{t}$CK (AVG) MIN.
12. The clock's $_{t}$CH (AVG) and $_{t}$CL (AVG) are the average half clock period over any 200 con- secutive clocks and is the smallest clock half period allowed, with the exception of a de- viation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.

13. The period jitter (t_{JITper}) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. t_{CH} (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. t_{CL} (ABS) is the absolute instantaneous clock low pulse width as measured from one fall- ing edge to the following rising edge.
16. The cycle-to-cycle jitter t_{JITcc} is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error $t_{ERRnper}$, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.
18. t_{DS} (base) and t_{DH} (base) values are for a single-ended 1 V/ns slew rate DQs (DQs are at 2V/ns for DDR3-1866) and 2 V/ns slew rate differential DQS, DQS#; when DQ single- ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transi- tion edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (towhich derating tables apply) to V_{REF} when the slew rate is 1 V/ns (DQs are at 2V/ns for DDR3-1866). These values, witha slew rate of 1 V/ns (DQs are at 2V/ns for DDR3-1866), are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual t_{JITper} (larger of t_{JITper} (MIN) or t_{JITper} (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output pa- rameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The fol- lowing parameters are required to be derated by subtracting $t_{ERR10per}$ (MAX): t_{DQSCK} (MIN), t_{LZDQS} (MIN), t_{LZDQ} (MIN), and t_{AON} (MIN). The following parameters are re- quired to be derated by subtracting $t_{ERR10per}$ (MIN): t_{DQSCK} (MAX), t_{HZ} (MAX), t_{LZDQS} (MAX), t_{LZDQ} (MAX), and t_{AON} (MAX). The parameter t_{RPRE} (MIN) is derated by sub- tracting t_{JITper} (MAX), while t_{RPRE} (MAX) is derated by subtracting t_{JITper} (MIN).
24. The maximum preamble is bound by t_{LZDQS} (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its re- spective clock signal (CK, CKB) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The t_{DQSCK} (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by t_{HZDQS} (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT com- mands. In addition, after any change of latency t_{XPDLL}, timing must be met.
29. t_{IS} (base) and t_{IH} (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CKB differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CKB) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold

times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.

31. For these parameters, the DDR3L SDRAM device supports $_{t}$*n*PARAM (*n*CK) = RU($_{t}$PARAM [ns]/$_{t}$CK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For exam- ple, the device will support $_{t}$*n*RP (*n*CK) = RU($_{t}$RP/$_{t}$CK[AVG]) if all input clock jitter specifi- cations are met. This means that for DDR3-800 6-6-6, of which $_{t}$RP = 5ns, the device will support $_{t}$*n*RP = RU($_{t}$RP/$_{t}$CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the in- ternal PRECHARGE command until $_{t}$RAS (MIN) has beensatisfied.
33. When operating in DLL disable mode, the greater of 5CK or 15ns is satisfied for $_{t}$WR.
34. The start of the write recovery time is defined as follows: • For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    a. For BC4 (OTF): Rising clock edge four clock cycles after WL
    b. For BC4 (fixed by MRS): Rising clock edge two clock cycles afterWL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in exces- sive current, depending on busactivity.
36. The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an aver- age refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When T_C is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when $_{t}$REFPDEN (MIN) is satisfied, there are cases where additional time such as $_{t}$XPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown. This output load is used for ODT timings.Designs that were created prior to JEDEC tightening the maxi- mum limit from 9ns to 8.5ns will be allowed to have a 9nsmaximum.
39. Half-clock output parameters must be derated by the actual $_{t}$ERR10per and $_{t}$JITdtywhen input clock jitter is present. This results in each parameter becoming larger. Theparame- ters $_{t}$ADC (MIN) and $_{t}$AOF (MIN) are each required to be derated by subtracting both $_{t}$ERR10per (MAX) and $_{t}$JITdty (MAX). The parameters $_{t}$ADC (MAX) and $_{t}$AOF (MAX) are required to be derated by subtracting both $_{t}$ERR10per (MAX) and $_{t}$JITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn- off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown. This output load is used for ODT timings.
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than $_{t}$RFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Ad- ditionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate ac- cesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level

must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

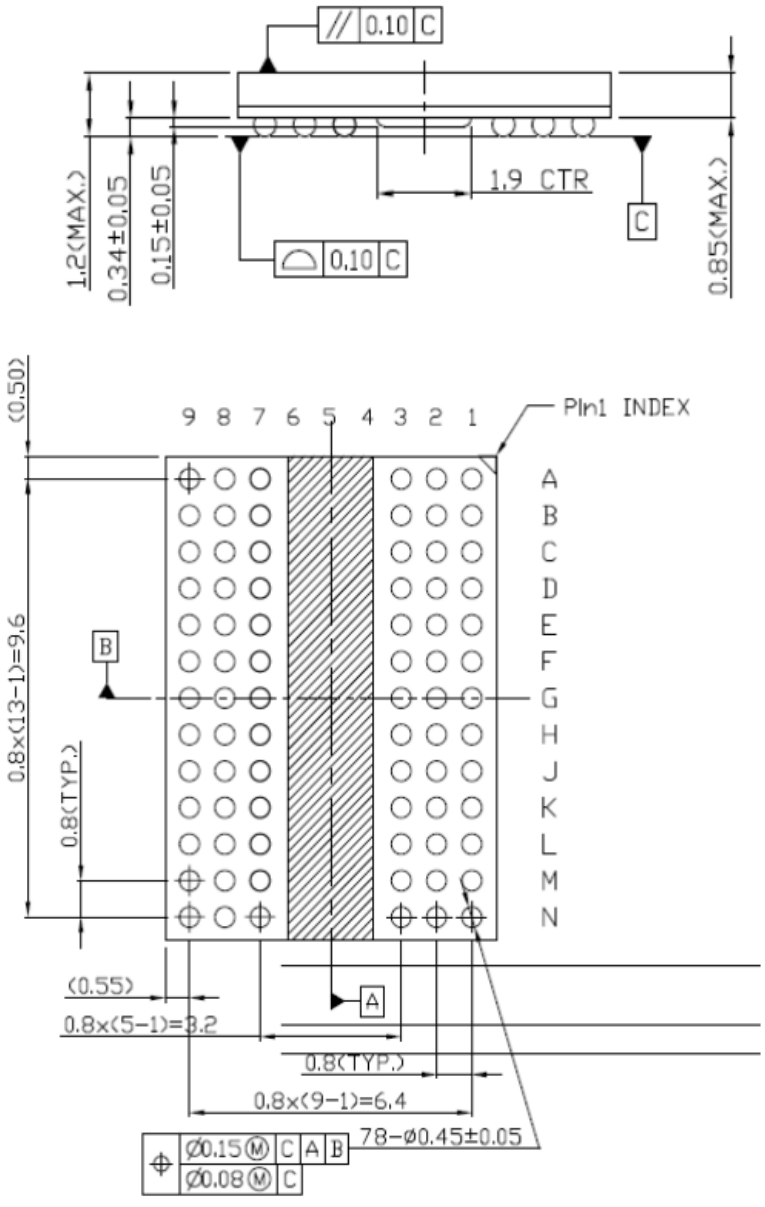
For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/ command inputs must use either $V_{IH(AC175),min}$ with $_{t}$IS(AC175) of 200ps or $V_{IH(AC150),min}$ with $_{t}$IS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with $_{t}$DS(AC175) of 75ps or $V_{IH(AC150),min}$ with $_{t}$DS(AC150) of 125ps.

8 Package Outlines

Figure 3 reflects the current status of the outline dimensions of the DDR3L packages for 2Gbit components x8 configuration.

Figure 3 - Package outline

FBGA78 x8



9 Product Type Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter

Table 7 - DDR4 Memory Components

Field	Description	Values	Coding
1	UniIC Component Prefix	SCB	UniIC
2	Voltage	13	VDD, VDDQ=1.35V
3	DRAM Technology	H	DDR3
4	Density	2G	42Gbit
5	Number of I/Os	80	x8
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
8	Package,	F	FBGA
9	Power	–	Standard power product
		L	Low power product
10	Speed Grade	11M	CL–tRCD–tRP = 13-13-13
		13K	CL–tRCD–tRP = 11-11-11

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